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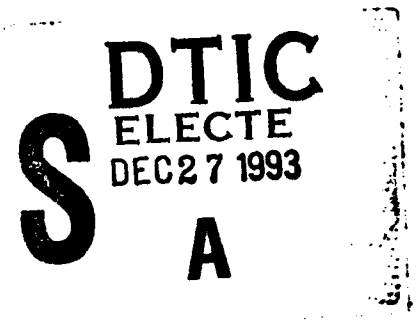

Development of a 4-bit Parallel Analog-to-Digital Converter and a Four-Quadrant Double-Balanced Mixer Using Heterojunction Bipolar Transistor Technology

THESIS

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THESIS

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Abstract

A 4-bit parallel analog-to-digital converter (ADC) and a four-quadrant double-balanced mixer were designed and simulated using heterojunction bipolar transistor (HBT) technology to test the dc and high-frequency characteristics of HBTs. HSPICE simulations of small-scale components and the large-scale ADC operated within expected ranges. The ADC implemented with the Rockwell HBT model operated at a sampling rate of over 1 GHz, and the Fellows model also operated at a 1 GHz sampling rate. The mixer produced an intermediate frequency (IF) signal using radio frequency (RF) and local oscillator (LO) inputs. The circuit produced a +9 dB power gain with less than one percent harmonic distortion and shows potential for microwave applications.

In order to facilitate the fabrication of HBT circuits, a Magic technology file was developed to lay out HBTs and extract the transistors for the purpose of doing a layout versus schematic check. The extraction software was altered to recognize HBTs in the extracted file. The program ext2spice successfully identified HBTs and converted the transistors, as well as parasitic capacitances, into an HSPICE netlist. Since load resistors determine the output logic swing in current-mode logic, an attempt was made to extract resistors using the HBT technology file for Magic. The configuration of the HBT within Magic and the methods used for resistance extraction offer ways to extract HSPICE netlists for accurate simulations.

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I. Introduction

1.1 Background

Since the inception of the first bipolar junction transistor (BJT) in 1947, there has been a strong drive to increase the power, efficiency, and versatility of this cornerstone of the electronic circuit industry. In 1957, Kroemer introduced the theories behind the higher emitter efficiency and higher frequency capabilities of heterostructure bipolar devices [1]. Kroemer's theories built the foundation for research involving what is known today as the heterojunction bipolar transistor.

While current technologies produce predictable, high yield results, there are several inherent disadvantages that are not present in HBTs. Although complementary metal-oxide-semiconductor (CMOS) devices produced on silicon substrates currently dominate the very large scale integrated (VLSI) circuit industry, CMOS does not offer the current drive capabilities that bipolar devices offer. Also, complementary transistor technology does not have the same advantages on gallium arsenide (GaAs) substrates as on silicon due to two main reasons. The first reason concerns the fact that the advantage of high electron mobility in GaAs is negated by a lower mobility of holes ($\mu_{nGaAs} >> \mu_{pGaAs}$) which neutralizes the advantages of implementing both n-channel and p-channel field effect transistors on a single GaAs wafer. The other problem that GaAs technology exhibits is the inability to grow a quality oxide on GaAs substrates, which does not permit the growth of oxide layers for gates such as MOS transistors. The heterojunction bipolar transistor provides greater current drive capabilities and faster operational components than existing CMOS and GaAs field effect transistor technologies, while circumventing the disadvantages of these technologies.

Another important trend in HBT technology is the improved reliability in the fabrication process of the transistor. Consistent molecular beam epitaxy (MBE) processes, which allow for the precision growth of atomic layers on semiconductor substrates, have brought better performance and reliability to the HBT field [2]. Also, through self-aligned base contacts, better passivation techniques, and precisely grown vertical structures, the performance characteristics of the HBTs have been improved [3]. These factors provide HBT technology advantages of increased operational frequencies, higher efficiencies, and size reduction over other technologies [4,5] .

A number of digital circuits were produced in the last ten years using AlGaAs/GaAs HBTs, such as frequency dividers [6], high-speed gate arrays [7], and multiplexers [8]. This push for state-of-the-art electronic components has called for the development of highly accurate modeling tools to simulate the operation of simple heterostructure devices, as well as more complex HBT circuits. Rockwell International has adapted a BJT HSPICE model for HBT simulations, which accurately models the dc electrical characteristics. Rockwell has collaborated with the Air Force Wright Laboratory on HBT research efforts concerning analog-to-digital converters with moderate success [9]. With the recent success in the HBT research field, there is a growing need for accurate simulation tools and efficient mask layout capabilities for circuit designers.

1.2 Problem Statement

The implementation of integrated circuits using HBT technology required the development of a HSPICE model that accurately simulated an active HBT device and the modification of or access to a mask layout editor to implement layouts of new fabrication techniques. The problem that this research effort attempted to solve is the design of small-scale circuits using HBT technology, so that HBT research can begin at the Air Force

Institute of Technology (AFIT). This facilitates the development of high-speed digital and analog circuits.

1.3 Objectives

The objective of this thesis was to design and simulate the components of small-scale integrated circuits implemented using HBT technology. The circuits that were designed and simulated are the components of a 4-bit parallel analog-to-digital converter (ADC) and a four-quadrant analog mixer/multiplier. The ADC tested the dc performance of the HBT transistor for both analog and digital applications. The mixer/multiplier tested the high-frequency response of the HBT. Since the Wright Laboratory HBTs are designed for high-power microwave applications, the mixer/multiplier was chosen specifically to investigate the Wright Laboratory HBTs.

An ADC with parallel configuration consists of a sample-and-hold unit, comparators, NOR/OR gates, and an encoding stage (OR gates). A simplified schematic can be seen in Figure 1. The output latches are part of the encoding stage.

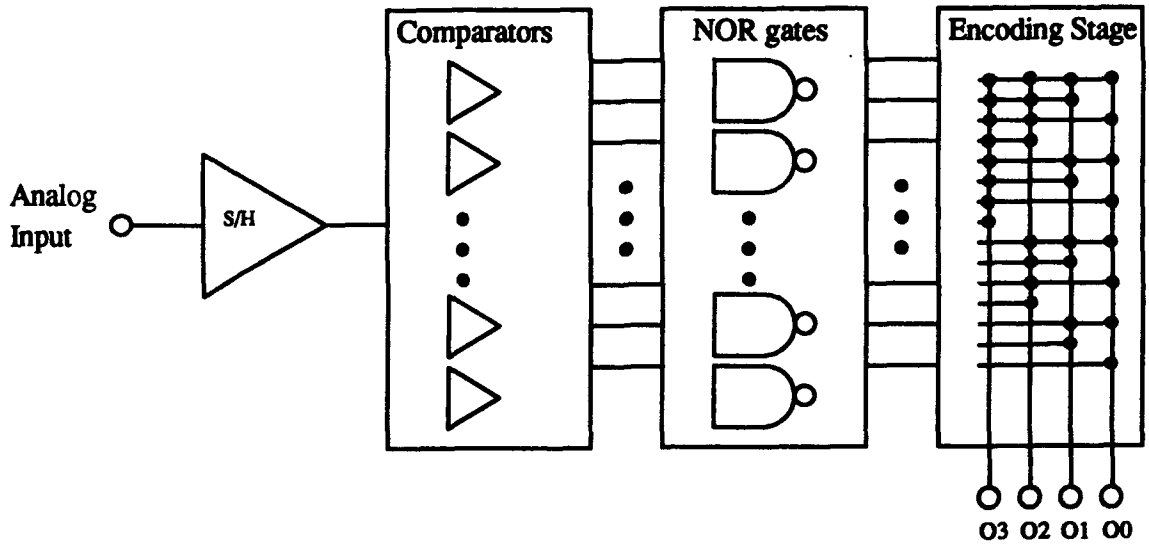


Figure 1. Simplified operational schematic of a parallel ADC.

A simplified operational schematic of the mixer/multiplier is shown in Figure 2. This figure shows the inverse-hyperbolic tangent component that gives the mixer its four-quadrant operational capabilities.

The primary focus of the objective was to select an accurate HSPICE model to predict circuit performance, and use an available mask layout editor that will enable implementation of mask layouts of HBTs using current fabrication techniques. Capabilities exist for circuit extraction in several layout editors, so the code can be altered to incorporate vertical HBTs and achieve accurate HSPICE netlist representations including parasitic capacitances, resistances, and other electrical and timing properties. These extracted circuits are to be checked for proper connectivity and resimulated with the associated parasitics.

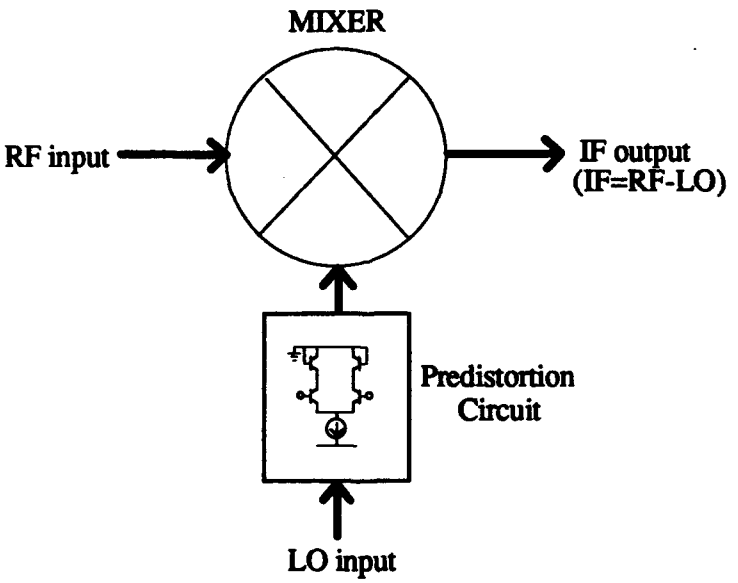


Figure 2. Simplified operational schematic of an analog mixer/multiplier.

1.4 Approach

The problem was approached in four steps: HSPICE model selection, mask layout development, small-scale design and simulation of ADC components and mixer, and large-scale ADC design and simulation. These steps are detailed in the following sections.

1.4.1 HSPICE Model Selection. An accurate HSPICE model was crucial for the success of this project. There are currently several variations of a modified Gummel-Poon BJT model emulating HBT characteristics [3,4,9]. However, most of these models do not reflect the current fabrication techniques and recent advances achieved in transistor fabrication processes. While Wright Laboratory has a new HBT fabrication process that promises to have improved performance parameters, their focus is on high-power transistors for microwave applications. The ADC project does not require the larger transistors needed for microwave applications, but the mixer is a good candidate for insertion of the Wright Laboratory HBT. Fellows has developed a new physics-based model for the Wright Laboratory HBT [10]. While Fellows has accurately modeled several versions of the Wright Laboratory HBT, this thesis is concerned with the model for the baseline one-finger, one-dot, three-micron diameter geometry. Rockwell also provided an adapted BJT parameter model for transistors that are smaller and built for more general-purpose applications. Between the Fellows model and the Rockwell model, the requirement for an accurate HSPICE HBT model has been met.

1.4.2 Mask Layout Development. AFIT currently has a mask layout editor called Magic which uses a technology file to interpret and transform mask layers into active devices, as well as parasitic capacitances and resistances. The scalable CMOS (SCMOS) version of the technology file is a well-developed technology file that has been used in the AFIT VLSI Laboratory. This file has provided important information on how to develop a technology file that will have the capabilities of extracting vertical HBTs and the parasitics involved in interconnects.

While lateral BJTs have been implemented in Magic in the past, vertical BJTs have not been implemented based on the surveyed literature. Because HBTs consist of vertical structures, it is difficult to create a technology file that will interpret HBT configurations. Another problem that has surfaced is the inability of Magic to create non-Manhattan

geometries (i.e. arcs, trapezoids) such as dot emitters which are present in current HBT configurations at Rockwell and Wright Laboratory. However, rectangular and square geometries can be implemented in Magic and translated into either Caltech Intermediate Format (CIF) or GDS-II format. These formats could be interpreted by another mask layout editor with non-Manhattan geometry capabilities to finish transistor details with little effort. Due to the limitations of Magic, Wright Laboratory offered the use of their layout editor, DW2000, as an alternate route for finishing the details of the Wright Laboratory baseline transistor.

The extraction capabilities of the SCMOS technology file are explicitly limited to MOS transistors. Although there are no provisions for extracting bipolar transistors, there existed the possibility that the extractor could be fooled into thinking that a dummy HBT in a layout is a MOS transistor with drain, gate, source, and substrate terminals which would actually be the collector, base, emitter, and substrate terminals in the real layout. The extracted netlist would be translated into a HSPICE implementation using an adapted version of the *ext2spice* conversion program.

1.4.3 Small-scale Component Design and Testing. The two predominant HBT logic families that are in use today are the emitter coupled logic (ECL) family and the integrated injected logic (I^2L) family, which are shown in Figure 3 and Figure 4 [11]. While the I^2L circuits consume less area per integrated circuit, they are slower than ECL configurations because the current source transistor is allowed to saturate and store charge. The stored charge slows the transition of the transistor to the off state. ECL is built using differential pairs and can be operated so that the transistors are not allowed to saturate. Because integrated circuits developed using HBT technology focus on high-speed applications, the ECL configurations are more attractive even though they consume more area on the integrated circuit.

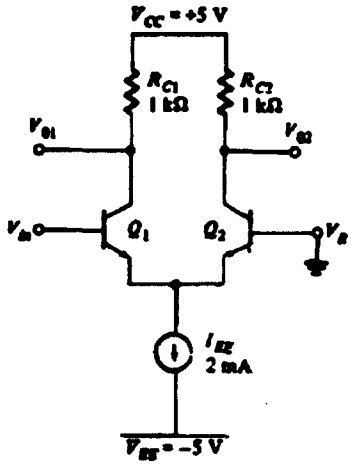


Figure 3. A simple current switch using ECL logic [11].

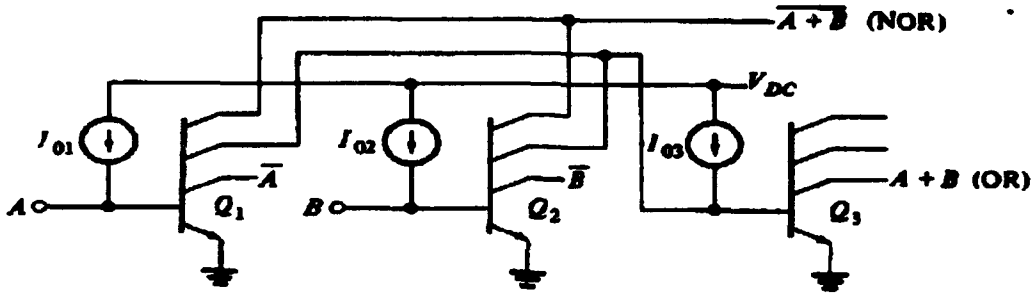


Figure 4. A NOR gate implemented using I^2L [11].

Comparators, sample-and-hold units, and NOR/OR gates are all integral parts of analog-to-digital converters. Each of these individual components were implemented using ECL logic. The small-scale circuits were first simulated using HSPICE to obtain timing characteristics such as propagation delay, and electrical properties such as power consumption for each circuit. The transistors were not allowed to enter the saturation region. To have the transistors biased in the saturation mode would slow down the high-speed performance of the circuits dramatically.

The mixer was a small circuit that contained under 100 transistors. The circuit was based on balanced HBT pairs. This eased research efforts somewhat, because the comparators and NOR/OR gates were based on differential pairs as well.

Once the HSPICE netlists for the subcircuits were tested, the small-scale components were implemented as mask layouts and an attempt was made to extract the transistors, as well as parasitic capacitances and resistances.

1.4.4 Large-scale Design and Simultation. The individual component netlists for the ADC were then incorporated into a single netlist as subcomponents and simulated using HSPICE for proper operational characteristics and to find electrical and timing properties for the ADC. Also, the high-frequency performance of the mixer was analyzed by determining the output gain and other performance parameters. At this point, the results of the electrical and timing characteristics were compared to components that have been developed in previous research efforts. This was done to expose speed or power advantages using the available HSPICE models. The large-scale ADC was implemented in Magic and then translated into a GDS-II or CIF mask layout file format for the purpose of implementing accurate HBT geometries.

1.5 Thesis Overview

The following chapters present a literature review of previous research efforts, as well as the procedures and results of this thesis effort. Chapter II presents the theory behind the increased efficiency and improved performance parameters of the HBT, so that an appreciation can be obtained for HBT technology and its figures of merit. Chapter III presents a summary of the literature review, and provides performance characteristics for previous HBT research efforts. Chapter III also presents applications for HBT technology. Chapter IV presents the design and simulation steps of the components of the 4-bit ADC and mixer and alterations to the Magic technology file and extraction code.

Chapter V presents the results of simulation and layout of the circuits designed in the previous chapter. Chapter VI is the summary of the thesis, conclusions of the designs advantages and disadvantages, and recommendations for future HBT designs.

II. Heterojunction Bipolar Transistor Theory

This chapter contains the theory behind the high-speed performance of HBTs. It also offers an insight on the advantages of the HBTs dc and high-frequency figures of merit in terms of fabrication techniques, device geometries, and material characteristics. This section shows that HBTs offer advantages in circuit implementation over GaAs MESFET and conventional bipolar implementations.

2.1 Emitter Efficiency Theory

The theory that first suggested heterostructure bipolar devices was published in 1957 by Kroemer [1]. This theory was based on the idea that a wide band gap at the emitter-base junction would increase the carrier efficiency flowing from the emitter into the base. This has been proven by looking at the current equations for a bipolar transistor. The various components of current contributors in a typical p-n-p transistor biased in the forward active mode are shown in Figure 5 [12].

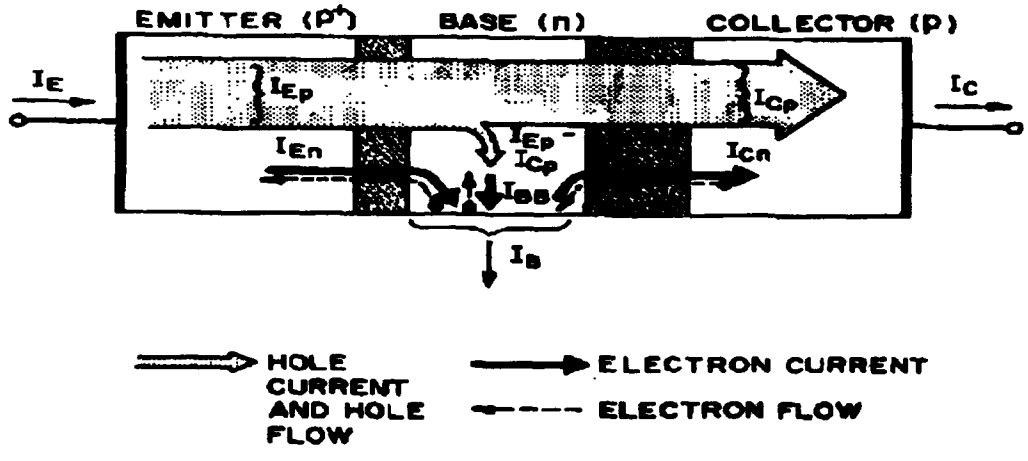


Figure 5. Current components for electrons and holes in a p-n-p BJT [12].

The common-emitter current gain, β_O, is found by (1) where α_O is the common-base current gain.

$$\beta_o = \frac{\alpha_o}{1-\alpha_o} \tag{1}$$

The common-base current gain can be represented as (2).

$$\alpha_o = \frac{I_{Cp}}{I_E} = \frac{I_{Cp}}{I_{Ep}+I_{En}} = \frac{I_{Ep}}{I_{Ep}+I_{En}} \cdot \frac{I_{Cp}}{I_{Ep}} \tag{2}$$

The current components in (2) which effect the emitter efficiency are the injected hole current, I_{Ep}, exiting the emitter and entering the base, the electron current, I_{En}, entering the emitter from the base, and the total emitter current, I_E. The hole current will reach the collector after crossing the base. This creates a hole current in the collector, I_{Cp}, if the lifetime of the carrier in the base is longer than the transit time across the base.

The common-base current gain is separated into two components in (3), the emitter efficiency, γ, which is the ratio of injected hole current to the total emitter current, and the base transport factor, α_T, which is the ratio of hole current reaching the collector to the hole current injected from the emitter.

$$\alpha_o = \gamma \cdot \alpha_T \tag{3}$$

Both γ and α_T are given in (4) and (5), respectively.

$$\gamma = \frac{I_{Ep}}{I_{Ep}+I_{En}} = \frac{1}{1+\left(\frac{I_{En}}{I_{Ep}}\right)} \tag{4}$$

$$\alpha_T = \frac{I_{Cp}}{I_{Ep}} \tag{5}$$

In order to increase the base transport factor, a thin base is commonly used to ensure that most of the injected hole current reaches the collector. In order to increase the emitter efficiency, the parasitic component I_{En} should be reduced by either doping the emitter more heavily, or by using a heterojunction, which will be developed in this chapter.

In order to develop the theory behind an emitter efficiency increase, the equations for a simple p-n junction at the emitter-base contact must be examined. The simple diode equations for I_{En}, and I_{Ep} are shown as a ratio between the electron and hole currents at the emitter-base junction in (6). The current ratio represents the controlling component in the emitter efficiency equation.

$$\frac{I_{En}}{I_{Ep}} = \frac{(qD_{nE}n_{oE}/L_{nE})\cdot(e^{\frac{V}{V_t}}-1)}{(qD_{pB}n_{oB}/L_{pB})\cdot(e^{\frac{V}{V_t}}-1)} = \frac{D_{nE}L_{pB}n_{oE}}{D_{pB}L_{nE}n_{oB}} \tag{6}$$

The efficiency is dependent on the diffusion constants for electrons in the emitter, D_{nE}, and holes in the base, D_{pB}, the diffusion lengths for electrons in the base, L_{nB}, and holes in the emitter, L_{pE}, and the equilibrium minority carrier concentrations for holes in the base, p_{oB}, and electrons in the emitter, n_{oE}. The efficiency is independent of the applied voltage across the junction, V, and the thermal voltage, V_t. Since the diffusion constants and lengths are fixed material constants, the most significant contributor to emitter efficiency is the equilibrium minority carrier concentration.

The mass action law gives relationships between the equilibrium minority carrier concentrations and the intrinsic carrier concentrations in the emitter in (7), and in the base in (8).

$$n_{oE} = \frac{n_{iE}^2}{N_E} \tag{7}$$

$$n_{oB} = \frac{n_{iB}^2}{N_B} \tag{8}$$

The net acceptor density in the emitter, N_E, and the net donor density in base, N_B, are doping parameters, which are constant for a specific process. The intrinsic carrier concentration for the base, n_{iB}, and for the emitter, n_{iE}, can be found from (9).

$$n_i^2 = N_C N_V \cdot e^{-E_g/kT} = 4\left[\frac{2\pi kT}{h^2}\right]^3 (m_p^* m_n^*)^{3/2} \cdot e^{-E_g/kT} \tag{9}$$

N_C and N_V are the effective density of states for the conduction and valence bands, respectively, k is Boltzmann's constant, T is the temperature, h is Planck's constant, m^*_n and m^*_p are the effective masses of the electrons and holes, respectively, and the energy gap of the material is given by E_g.

The ratio of the carrier concentrations, n_{iE} to n_{iB}, can be expressed in the form of (10), which shows that the intrinsic carrier concentration ratio is dependent on the effective masses of the electron, m^*_{nE},and hole, m^*_{pE}, in the emitter, and electron, m^*_{nB}, and hole, m^*_{pB}, in the base, and the difference between energy gaps, ΔE_g, between the base and emitter.

$$\frac{n_{iE}^2}{n_{iB}^2} = \left(\frac{m_{pE}^* m_{nE}^*}{m_{pB}^* m_{nB}^*}\right)^{3/2} \cdot e^{-\Delta E_g/kT} \tag{10}$$

Therefore, the ratio of the electron current to hole current reduces to the form expressed in (11), where the dominant component is the exponential factor, considering the effective masses to be nearly equal.

$$\frac{I_{En}}{I_{Ep}} = \frac{D_{nE} L_{pB} N_B}{D_{pB} L_{nE} N_E} \left(\frac{m_{pE}^* m_{nE}^*}{m_{pB}^* m_{nB}^*}\right)^{3/2} \cdot e^{-\Delta E_g/kT} \tag{11}$$

If AlGaAs and GaAs are considered as potential materials for the emitter and the base, respectively, the electron to hole current ratio is 1:1500, as depicted in Table 1, and the emitter efficiency approaches one. If the transistor is designed so that the base

transport factor is also close to one, the common-base gain approaches one. This will allow the common-emitter current gain in (1) to increase to a value of several hundred. It will be shown later that this high gain is not as useful in itself, but can be sacrificed to reduce parasitic effects in the HBT.

Table 1. The effect of a heterojunction on the emitter efficiency of an AlGaAs/GaAs HBT.

Component	Effect
ΔEg	0.19 eV
$-\Delta Eg/kT$	-7.31
$\exp(-\Delta Eg/kT)$	1/1500

2.2 Process Characteristics

A common implementation of the HBT consists of the n-p-n AlGaAs/GaAs vertical HBT. Different baseline processes have been presented in several articles [3,4,9]. An energy band diagram of an unbiased n-p-n HBT is shown in Figure 6. The corresponding cross-section of an AlGaAs/GaAs emitter-up vertical HBT is shown in Figure 7.

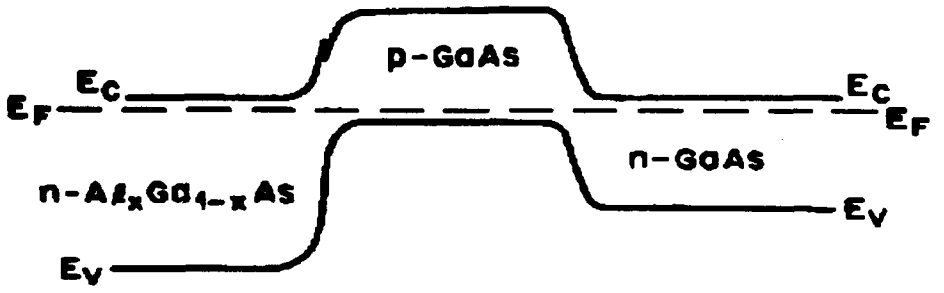


Figure 6. Energy band diagram of an unbiased n-p-n HBT [12].

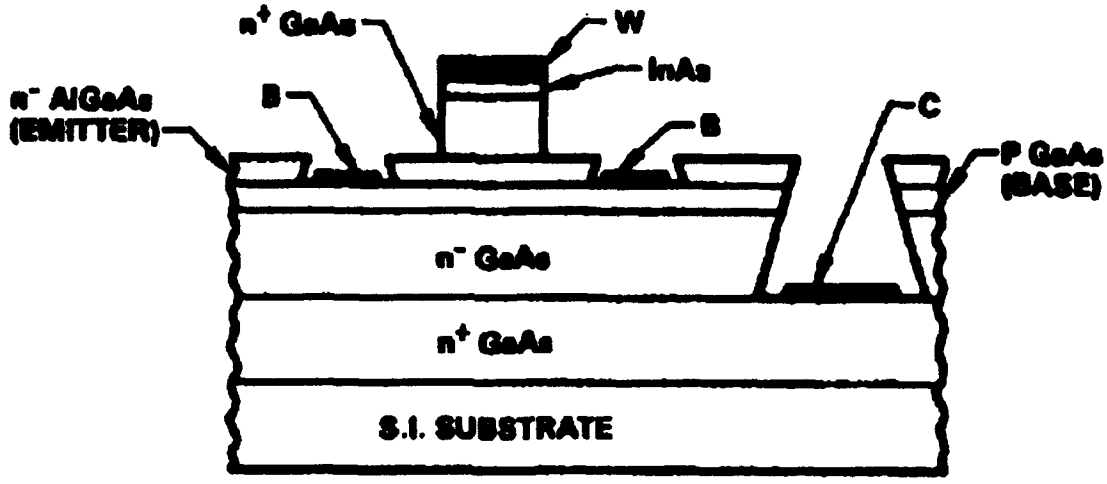


Figure 7. Vertical structure of a typical n-p-n HBT [9].

The band gap difference between the emitter and base allow other adjustments to be made to the doping profile of the HBT. First, the emitter efficiency is strongly dependent upon N_B, N_E, and ΔE_g. Substituting (11) into (4), the emitter efficiency is obtained in (12).

$$\gamma \cong \frac{1}{1+\frac{D_{nE}L_{pB}N_B}{D_{pB}L_{nE}N_E}\left(\frac{m_{pE}^{*}m_{nE}^{*}}{m_{pB}^{*}m_{nB}^{*}}\right)^{3/2}\cdot e^{-\Delta E_g/kT}} \tag{12}$$

The base doping can be increased, since it is compensated for by the exponential dependence on ΔE_g. An increase in base doping in a homojunction BJT would not improve performance, since the emitter efficiency would be reduced. The increase of N_B in an HBT decreases the resistivity of the base and can be seen by examining the relationship between resistivity and doping in an n-p-n transistor in (13). The reduction of base resistance is accomplished without a decrease in the efficiency of the HBT.

$$\rho = \frac{1}{q\cdot\mu_n\cdot N_B} \tag{13}$$

A decrease in the resistivity of the base will allow the minority carrier to cross the base in less time. This will speed up the response time of the transistor.

The complement to the n-p-n transistor is the p-n-p transistor, which is appealing for the low base resistance due to a thin epitaxially grown n-type layer. The applications for the p-n-p transistor are limited, however, since the p-type regions increase the emitter and collector resistance, as well as increase the base transit time due to the lower mobility of the holes. The only function that may be operationally feasible for the p-n-p HBT is its complementary use as an active load, current source, or push-pull amplifier. Other compounds have been investigated for heterostructure bipolar devices, but the fabrication process is still in the initial stages and will have to mature before implementation is practical. The InP/InAlGaAs combination shows promise [13], as well as the Si/SiGe combination [14].

2.3 DC Characteristics

The dc characteristics of the AlGaAs/GaAs HBT exhibit several advantages over other technologies such as high transconductance, reduced base width modulation, device uniformity, high current gains, high breakdown voltages, and improved radiation hardness. These advantages will be defined and compared with other technologies within this section.

The first advantage over MESFETs is a higher transconductance, g_m, which varies according to the output current. The transconductance of a bipolar junction transistor is defined in (14).

$$g_m = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{V_{CE}=\text{constant}} \tag{14}$$

The high transconductance is due to the exponential dependence of the output collector current , I_C, on the input voltage , V_{BE}, across the base-emitter junction of the transistor. This can be derived by taking the partial derivative of the collector current in (15) with respect to the input voltage with the voltage across the collector-emitter junction, V_{CE}, held constant. The constants a_{21} and a_{22} are coefficients calculated from material constants, device geometries, and doping parameters [12].

$$I_C = a_{21}(\exp^{\frac{V_{BE}}{V_t}} - 1) + a_{22} \tag{15}$$

A high transconductance in the HBT allows a small input voltage swing to produce high output voltage gains. The output drain current in a MESFET has, at best, a quadratic dependence on the input gate voltage, V_G, in the saturation region. The transconductance of a MESFET can be determined using (16).

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}} \tag{16}$$

The equation for drain current, I_D, in saturation is shown in (17), where C_o is a constant coefficient based on material properties and device geometries. The drain current is dependent on the applied gate voltage, V_G, and the threshold voltage, V_T. V_T is dependent on the built-in voltage of the metal-semiconductor junction and the pinch-off voltage of the MESFET [12].

$$I_{Dsat} = C_o (V_g - V_t)^2 \tag{17}$$

Therefore, larger current differentials can be obtained in the HBT with small voltage changes across the junctions of the transistor due to the exponential dependence of the output collector current to the base-emitter input voltage.

The high current transconductance also offers benefits over typical silicon bipolar junction transistors. One benefit is the reduction of high injection and Kirk effects. The Kirk effect is noticed in bipolar devices with lightly doped collectors. Under high current conditions, the high-field region across the base-collector junction is moved to the opposite end of the collector at the n-n^+ junction. This effectively pushes the base region out to W_B+W_C as shown in Figure 8 [15]. HBTs reduce the chance of this occurring through the high base doping which keeps the high field region across the base-collector junction.

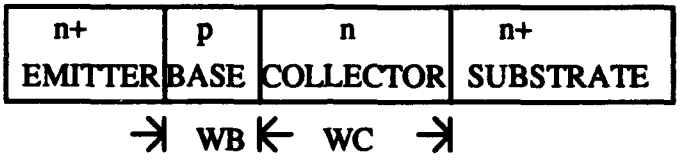


Figure 8. Kirk effect in an n-p-n BJT.

Another advantage of HBTs over BJTs is the minimization of base width modulation because of the highly doped base. This is due to the extensive amount of carriers available in the base, which minimizes the effective base width variation present in silicon BJTs. The formula for output conductance, g_o, is shown in (18). The Early voltage, V_A, is the extrapolated voltage on the I-V characteristics where the slopes of the I_C-V_{CE} curves intercept the negative V_{CE} axis.

$$g_o = \left.\frac{\partial I_C}{\partial V_{CE}}\right|_{V_{BE}=\text{constant}} \approx \frac{I_C}{V_A} \tag{18}$$

If the slope of the I_C-V_{CE} curve with a constant V_{BE} is small, the intercept of the collector current axis will approximate the value of I_C in the forward active region. Thus, a good approximation of the output conductance will be I_C/V_A, where I_C is the approximate value of the collector current at the intercept and in the forward active

region. If I_C is dependent on the base width as shown in (19) [12], and the base width is dependent on V_{CE} when base width modulation is present, the dependence of V_A on base width modulation can be seen in (20). K is a constant that filters out of the differentiation that contains process parameters, such as doping concentrations and diffusion constants. If the assumption is made that for small changes in V_{CE}, the base width modulation is small, the final result of (20) is valid.

$$I_C = \frac{2D_{pB}Q_B}{W_B^2} \tag{19}$$

$$V_A = \frac{I_C}{\frac{\partial I_C}{\partial V_{CE}}} = \frac{-K \cdot W_B}{\frac{\partial W_B}{\partial V_{CE}}} = -K \cdot W_B \left(\frac{\partial V_{CE}}{\partial W_B}\right) \tag{20}$$

The important aspect of (20) is the relationship between V_{CE} and W_B. Base width modulation does not effect HBTs due to the high base doping, so the partial derivative is large. A large Early voltage is therefore an indicator that base width modulation is not a dominant factor. True to the prediction, the Early voltage is around 800 V in some processes, which is several times greater than silicon BJTs [4]. The presence of channel length modulation within FETs, also known as the Early effect, prevents MESFETs from being used in analog applications due to the higher output conductance than bipolar devices. MESFETs have frequency dependent characteristics due to the output conductance being heavily influenced by trapping effects and surface channel-substrate leakage [4].

The third advantage that HBTs possess is the high degree of uniformity between devices. The turn-on voltage, V_{BE} , for an HBT is dependent on the energy gap of the materials, which is precisely controlled during epitaxial growth. This is shown in (21), where E_{gB} is the energy gap of the base, I_C is the collector current, A is the emitter-base junction area, and R_C is the parasitic resistance in the collector.

$$V_{BE} \approx \frac{E_{gB}}{q} + V_t \cdot \ln\left[\frac{N_B W_B I_C}{q D_{pB} N_C N_V A}\right] + R_C I_C \qquad (21)$$

This equation shows that at high collector currents, the $R_C I_C$ component dominates the turn-on voltage which indicates a strong dependence on parasitic resistance, while at low collector current values the energy gap value, E_{gB}, dominates. Wang performed an analysis of the output gain and offset voltage of single differential pairs on a wafer [9]. The consistent and reproducible process parameters give highly uniform devices that give as low as 4.3 percent standard deviation for voltage gain matching at approximately 200 or 46 dB, and a 1.7 mV standard deviation for offset voltage matching around a typical V_{CEon}=0.2-0.4 V. The equivalent parameter to HBT turn on voltage for MESFETs is the turn-on voltage, which is dependent on the pinch-off voltage. The pinch off voltage depends on the implant profile and thickness of the active channel, which is not as consistent as the MBE grown wafers and material characteristics in the HBTs.

Common-emitter current gain is one of the most important parameters and most flexible that the HBT possesses. The electron efficiency is improved dramatically by the large band gap of the emitter placed against the smaller band gap of the base for an n-p-n HBT [1]. The holes see a much larger barrier going into the emitter than the electrons see going into the base, which allows high dc current gains of several hundred to a thousand to be achieved. The high gain is not necessary, but by allowing the high gain to be compromised to moderate levels by doping the base heavily, the base resistance can be decreased. This allows a decrease in base transit time, which improves the transistor response.

Another high performance aspect of the HBT is the adjustable breakdown voltages across the junctions and the entire device. The breakdown voltage across the base-collector junction can be controlled through the width and doping level of the collector. Since the base is highly doped, the thicker and lower doped collector provides higher

breakdown voltages due to the avalanche process, but it also produces a larger effective transit time across the collector bulk. The emitter-base junction controls the current gain and is the most sensitive to reverse bias currents such as the Zener tunneling and avalanche processes which can damage the transistor. Due to this sensitivity, high breakdown voltage is required at the input comparators of the wide voltage range parallel A/D converter. This can largely be controlled by the emitter doping. The collector-emitter breakdown voltage is dependent largely on the base-collector breakdown voltage coupled with a feedback multiplication factor of the current gain when the base is driven by a current source [3]. The larger breakdown voltages across the device allow larger currents to flow through the active regions of the HBT.

2.4 High-frequency Characteristics

HBTs also show great promise for high-frequency microwave applications [4,16]. The high frequency characteristics of the HBT allows the transistor to play many roles in microwave technology today. Several figures of merit which are predominantly referenced in literature are detailed below.

The unity current gain cutoff frequency, f_T, corresponds to the frequency for which the current gain is equal to unity. f_T is given by a series of transit times across the device and contacts, as is shown in (22) for an n-p-n HBT [2].

$$f_T = \frac{1}{2\pi(\tau_{ee}+\tau_b+\tau_c+\tau_{cc})} \tag{22}$$

τ_b in (23) is the transit time for electrons across the base and has a quadratic dependence on the base width due to drift, as well as diffusion components. v_e is the electron velocity in the base, which is part of the drift component. The ability to grow thin base layers allows for small transit times through the base.

$$\tau_b = \frac{W_B^2}{2D_n} + \frac{W_B}{v_e} \tag{23}$$

τ_{ee} in (24) corresponds to the emitter-base charging time, where V_t/I_C represents the effective resistance and C_{BE} is the junction capacitance.

$$\tau_{ee} = \frac{V_t}{I_C} \cdot C_{BE} \tag{24}$$

The carriers stored in the emitter are negligible in heterojunction devices, but are significant in homojunction BJTs. τ_{ee} is directly proportional to the emitter-base capacitance and inversely proportional to the current through the collector. However, the increased electron efficiency due to the band gap barrier in the valence band of the emitter-base junction allows the doping concentration in the emitter to be reduced. This will decrease the capacitance at the emitter-base junction, thus l ring the emitter transit time according to the τ_{ee} equation. τ_c is dependent on complex velocity transport effects and not shown, and τ_{cc} in (25) is strongly dependent on the emitter, R_E, and collector, R_C, parasitic resistances. C_{CB} is the collector-base capacitance used to determine the collector charging time.

$$\tau_{cc} = (\frac{V_t}{I_C} + R_E + R_C)C_{CB} \tag{25}$$

Increasing the effective area of the emitter-base and base-collector junctions would decrease the resistance through each region, but would also cause an increase in the junction capacitances. Therefore, increasing the area for better current performance may have adverse effects on the parameters τ_{ee}, τ_{cc}, and τ_b.

Another parameter describing transistor performance is the maximum frequency of oscillation, f_{max}, under unity power gain. f_{max} is approximated by (26) [2]. The importance of a low base resistance can be examined from (26), where both the base

resistance, R_E, and the collector charging time, τ_{CC}, has a parabolic dependence on the maximum oscillation frequency.

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi \cdot R_B \cdot C_C}} \tag{26}$$

Another parameter that is important in high-frequency characterization is the device switching time constant, τ_S, which is described by (27) [4].

$$\tau_s \approx (5/2) \cdot R_B \cdot C_C + (\frac{R_B}{R_L})\tau_b + (3C_C + C_L)R_L \tag{27}$$

The direct dependence on the base resistance and the collector capacitance is evident, as well as a dependence on the load capacitance and resistance, C_L and R_L, respectively. By optimizing the R_BC_C time constant, a higher f_{max} and a lower τ_S can obtained, which will improve device performance for both high-frequency microwave and digital circuits.

Another high-frequency aspect of HBTs is the higher frequencies that are obtained as a result of easily grown thin epitaxial layers present in an HBT. The base width can be as low as several hundred angstroms thick with more relaxed lithography techniques required (1-3μm emitter) than for MESFETs, which require 0.2-0.5 μm geometries to achieve microwave frequencies [4].

It should be noted that many sacrifices dealing with device geometry can be made depending on the intended operation of the circuit. A thicker base can make the fabrication techniques simpler and reduces the base resistance, but increases the carrier transit time. This lowers f_T and f_{max} and decreases analog, as well as digital circuit performance. Also, the thicknesses of the emitter and collector can be increased to allow for larger breakdown voltages across their respective areas of the transistor. This will provide for better device protection against reverse currents, but again will increase the

transit time across the device. Device geometries are therefore tailored to suit the application and available processing capabilities.

2.5 Summary

The improved performance parameters of HBTs make the device a good candidate for future integrated circuit applications. This is due to improved emitter efficiency, which indirectly allows faster transit times through the base of the HBT. The AlGaAs/GaAs HBT exhibits superior dc characteristics, such as a higher transconductance, minimization of base width modulation, increased current gain, and adjustable breakdown voltages. The HBT also exhibits improved high-frequency performance with higher cutoff frequencies. The low base resistance increases the maximum frequency of oscillation, and provides for a low switching time constant. These advantages make the HBT a good device for the development of high-speed digital and high-frequency analog circuitry.

III. HBT Literature Review and Applications

The first articles detailing successes in implementing large scale circuits using HBT technology were published around 1986 [17,18]. Several articles appeared over the next few years exploring applications in which to apply this technology. This chapter of the thesis is intended to show some of the applications that have been researched using HBT technology, including ADCs and their components, multiplexers, gate arrays, toggle flip-flops, exclusive OR/NOR gates, and decision circuits as digital applications, and high-power amplifiers, microwave oscillators, mixer/multipliers, and optical receivers as high-frequency applications. This chapter will address these applications to summarize what type of research has preceded this effort.

3.1 Digital Applications

The HBT transistor incorporates many new advantages of modern fabrication technology into its process and theory. It is attractive for A-D conversion applications due to its high-speed and improved growing techniques which produce a uniform vertical structure. The disadvantages and advantages between HBT technology and silicon bipolar technology in ADC development have been explained in detail by Joy, *et al.* [19]. This reference shows a 2:1 sample rate advantage and a 1.5:1 large-signal analog bandwidth advantage of HBT technology over BJT technology. However, these advantages are gained at the expense of a 2:1 power consumption disadvantage. This reference also focuses on providing a large-signal analog bandwidth for the series-gated current-mode logic (CML) comparator which is commonly used in parallel ADCs.

A GaAs 4-bit parallel ADC was constructed using MESFET technology in 1986 by , Ducourant, *et al.* [20]. This effort was plagued with high defect density in the material, poor uniformity of the active layer doping profile, insufficient process control,

and surface parasitic effects at the channel-gate junction, resulting in varying and unstable I-V curves. The 4-bit ADC was successfully sampled at up to 3 GHz clock frequency.

The sample-and-hold (S/H) circuit at the input of the ADC helps maintain signal integrity at high input frequencies. The S/H function is to hold the analog input at a stable voltage while the signal propagates through the internal circuitry to the output. Accuracy and low distortion are two important performance parameters that must be examined in each S/H technology. The S/H components examined in this thesis effort were based on diode-bridge designs that appeared in several articles [18,21,22].

A high-performance sample-and-hold using AlGaAs/GaAs HBTs was reported by Gorman, *et al.* in 1987 [21]. This circuit contained 3 μm diameter dot-emitters, Schottky diodes, thin film resistors, and metal-insulator-metal (MIM) capacitors. The performance of this circuit specified track bandwidth (-3 dB), which is the bandwidth when the S/H is left in the track mode, of 1.8 GHz. The sampled-mode analog bandwidth is defined as the sample rate at which the amplitude of the output signal, using a Nyquist input signal, is 70 percent of the output amplitude at low frequencies. The Nyquist signal indicates the frequency of the input signal is half of the sampling frequency. The sampled-mode analog bandwidth was 400 MHz at a sample rate of 800 Ms/s. The low frequency distortion was a large improvement over GaAs MESFET technology, with the HBT implementation having the second and third harmonic distortions at less than -50 dBc for a 250 mV peak-to-peak output voltage amplitude. This research effort indicated that the technology for 8-bit accuracy in conversion systems up to 400 Ms/s was realizable using AlGaAs/GaAs HBTs.

The design for this S/H component is divided into three stages, an input buffer, a high-speed Schottky diode sampling bridge, and an output buffer. Buffers were also included at the clock inputs to the diode bridge to shift the differential emitter-coupled logic (ECL) compatible input and assure the proper interface with the diode-bridge [21]. While the actual wafer testing showed 1.8 GHz capabilities at the -3 dB bandwidth, the

SPICE simulation demonstrated a 2.5 GHz bandwidth for the S/H. The discrepancy was not accounted for in the paper, possibly due to processing or design issues. It is noted that HSPICE simulations during this thesis may also produce over-estimated findings.

An HBT implemented sample-and-hold circuit was reported by Poulton, *et al.*, in 1988 [22]. This design was chosen as the S/H component for the ADC implementation in this thesis and is detailed in Chapter IV. The performance characteristics for this circuit are a clock sample rate of 2 Gs/s with an analog input signal of up to 1 GHz. The implementation is basically the same as the previous S/H with a input buffer stage, the Schottky diode bridge, and the output buffer stage [22].

The most detailed presentation of a parallel ADC configuration was presented by Wang in 1989 [9]. This paper showed the series-gated comparator in detail and gave performance parameters for individual components. The digital components operated with a 4.5 V power-to-ground difference, a 1 mA HBT current source, and a 400 mV output logic swing. The SPICE parameters for Wang's baseline HBT process were used as a representative model until current parameters were available from Rockwell or Fellows. The designed components were a 4-bit quantizer and sample-and-hold unit. When output latches are added to the quantizer and the sample-and-hold unit, it becomes a parallel ADC. The quantizer contained a resistor ladder, 16 series-gated CML comparators, 2 and 3-input CML NOR gates, and an encoding stage with output buffers. The quantizer was operated at sampling speeds in excess of 1 Gs/s and demonstrated non-linear characteristics consistant with 8-bit accuracy.

Two other ADC techniques in addition to the parallel ADC were expressed in an article by de Graff in 1986 [18]. The first was a series-feedback (successive approximation) technique which uses a single comparator and requires one clock cycle per bit of conversion plus one or more additional cycles to allow for acquisition and settling time for the S/H. A simplified schematic of the series-feedback technique is shown in Figure 9. The single comparator actually makes this technique a better application for

MESFETs since there is no required device matching and the MESFETs have a high input impedance [18].

The other technique that was reported is the feed-forward or pipeline algorithm. It consists of a succession of quantizer/subtractor stages, each of which determines one or more bits of the conversion and passes a residue analog signal on to the next stage [18]. A simplified schematic of a the feed-forward configuration is shown in Figure 10.

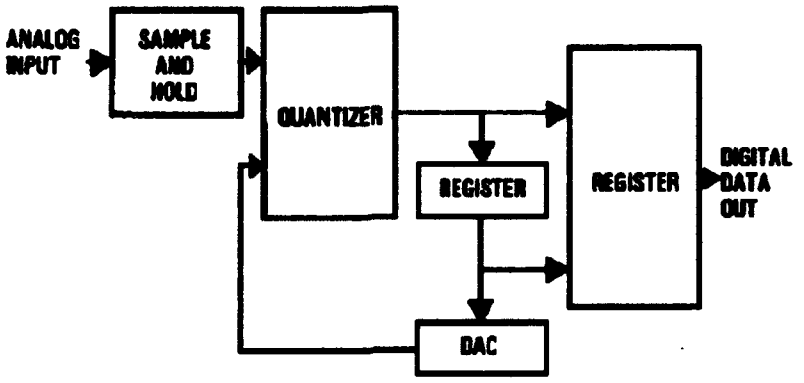


Figure 9. Simplified schematic of the series-feedback ADC configuration [18].

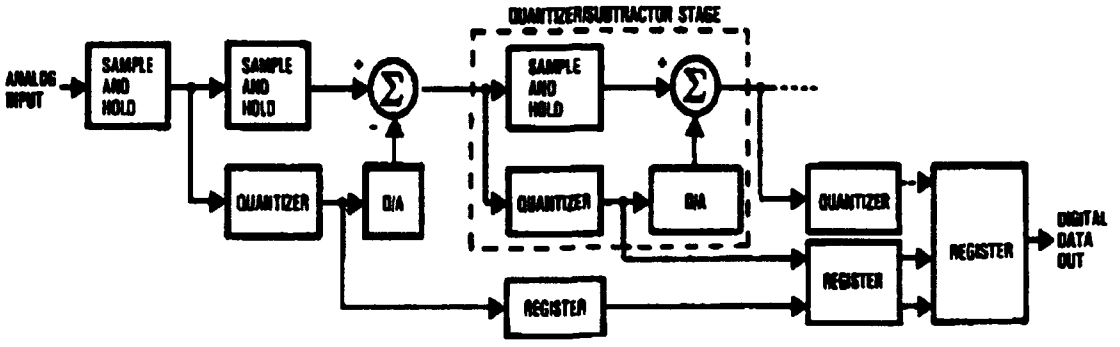


Figure 10. Simplified schematic of the feed-forward ADC configuration [18].

Digital components using HBT technology have been developed for future optical transmission systems in a research effort by Ichino in 1993 [23]. The components

researched within this article are a toggle flip-flop, a decision circuit, an exclusive NOR/OR gate, and a selector. These circuits operated with a 1 V input logic swing and a 1 V output logic swing. The toggle flip-flop was produced with short rise and fall times of 25 and 15 ps, respectively, with a 945 mW power consumption. The rise and fall times were measured using the 20 percent and 80 percent marks of the output with no load. Using the developed decision circuit, 20 Gb/s transmission was carried out with 1120 mW power consumption [24]. The exclusive NOR/OR gate performs differentiation and full-wave rectification of a pulse sequence in clock recovery circuits. Testing showed 20 Gb/s operational capabilities with 22 and 14 ps rise and fall times, respectively, and 700 mW power consumption. The selector circuit is a multiplexer which combines several parallel data channels to a single output for optical transmission. Performance characteristics were obtained at 20 Gb/s transmitting rate with 20 and 16 ps rise and fall times, respectively, and 1050 mW power consumption.

Emitter-coupled logic (ECL) is a popular logic family used for bipolar transistors, and HBTs have enjoyed a moderate amount of success using this family [23,24,25]. Combinational as well as sequential components have been designed using the series-gated current-mode logic (CML) configuration, which is related to ECL logic, but does not have emitter follower buffers at the output nodes as shown in Figure 11. The emitter buffers allow the circuit to drive following stages with higher current drive [26].

High-speed multiplexers were designed by Nubling, *et al.*, for high-speed fiber-optic communication applications using CML components implemented with HBTs [8]. This circuit used a 800 mV logic swing at the output and was capable of operating at data rates above 6 Gb/s. Each component consumed about 1.5 W. A high-speed gate array was implemented by Wang, *et al.*, in 1991 for integration into communication and instrumentation systems [27]. The basic logic gates consisted of CML circuits, and also provide for a divide-by-8 frequency divider. The gate array operated at over 15 GHz.

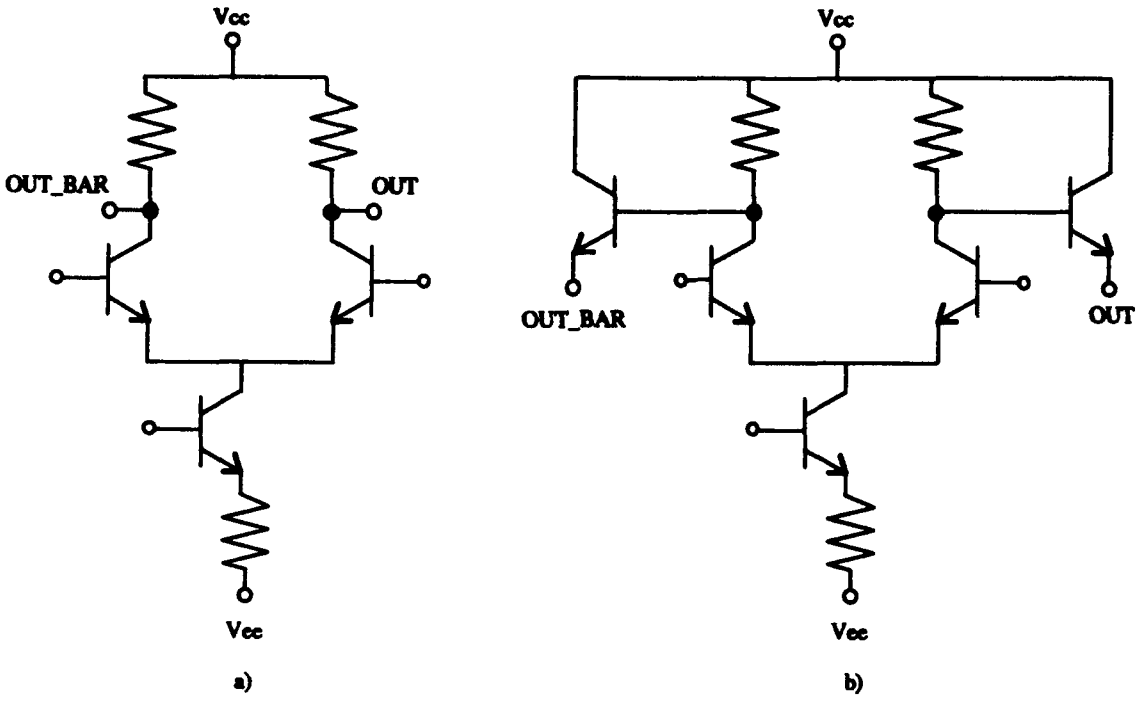


Figure 11. a) Current-mode logic (CML) and b) Emitter-coupled logic (ECL).

As a comparison, LaRue, *et al.*, reported FET-FET logic in 1990 using GaAs MESFETs to develop simple logic gates, such as the 3-input NOR gate [28]. These gates were able to achieve 200 ps propagation delays with approximately 1 mW of power being applied, a fan-out of 3, and a 125 fF capacitive load.

The series-gated CML configuration could be useful in implementing combinational circuitry such as ALUs, demultiplexors/multiplexors, or other combinational logic due to its flexibility. A RISC microprocessor is being developed at Rensselaer Polytechnic Institute using HBT technology and the components are being fabricated at Rockwell's Microelectronic Technology Center [29]. The research is developing a 1.0 GigaOPS RISC processor and a TeraOPS parallel processing application. Some of the components that are being built are an ALU carry chain, registers, a cache memory controller, and a clock deskew circuit which uses phased locked loops [29].

3.2 High-frequency Applications

The ability to epitaxially grow a narrow base a few hundred angstroms thick has provided easily obtainable high frequency devices with relaxed lithography techniques. HBTs possessing cutoff frequencies of over 100 GHz have been reported [30,31]. High output gain for circuits has also been an advantage in these devices.

High power microwave amplifiers have potential for using HBT technology considering its ability to sink high currents in small transistor areas and the presence of high breakdown voltages across the device area. Higgins reported high-efficiency X-band power amplifiers with 2-4 mW per μm of emitter length with 40-50 percent power-added efficiencies (PAE) [32]. Bayraktaroglu, *et al.*, reported in 1993 an HBT promising a dramatic performance increase in power efficiency over previous power transistors [33]. This is due to a heat spreading technique that controls internal device currents to avoid the occurrence of high current density areas. A record 10 mW per μm^2 power density was obtained at 10 GHz with 60 percent PAE. These transistors have applications toward transmitters and phased-array radar where power efficiency is crucial.

The relatively low $1/f$ noise associated with HBTs is due to the low phase noise. This has allowed microwave oscillators to be developed using the HBT technology with a much lower noise value than that implemented in GaAs FET technology [34]. The low $1/f$ noise benefits applications such as mixers and dividers where the baseband $1/f$ noise creates a high phase noise at the output [35].

Capabilities now exist to develop highly linear devices using HBTs due to the low output impedance associated with the high Early voltage, high transconductance, and the slow variation of dc current gain, β, to the collector current density, J_C. Because of these characteristics, linear amplifiers can be implemented with minimized harmonic distortion. A hybrid distributed amplifier has been developed using a $3x10\mu m^2$ HBT with a 10dB conversion gain at up to 9 GHz using less than 75 mW [36].

Also, in contrast to the high linearity capabilities, the HBT has the potential for nonlinear functions such as logarithmic amplifiers and mixers/multipliers by using the exponential relationship between the input voltage and the output current. High performance monolithic logrithmic IF amplifiers have been reported by Gorman, *et al.*, for applications with phased array antennas, electronic counter measure, sonar signal amplification, and power measurement [37]. These amplifiers boast a 60 dB dynamic range over 0.5 to 1.5 GHz [37]. A typical application for a high-frequency mixer is found in systems where RF signals are down-converted into an IF signal which can then be digitized by an ADC. A mixer was developed by Osafune, *et al.*, in 1991 that possessed a conversion gain of above +5 dB with I/O isolation of 33 dB up to 20 GHz [38].

3.3 Summary

This chapter presented a summary of previous research efforts involving HBTs and showed digital, as well as high-frequency, applications for HBT technology. Analog-to-digital conversion with a parallel configuration has been successfully employed in past research efforts using HBTs. Other digital components have been implemented with propagation delays, rise, and fall times on the order of tens of picoseconds, which is comparable to GaAs FET technology. HBT technology has several advantage over GaAs FETS for parallel A-D conversion including lower delay times and a higher degree of uniformity.

IV. Circuit Design and Procedures

This chapter details the procedures followed during the thesis effort. The procedures are divided into two sections, HSPICE circuit simulation and mask layout. Simulations and mask lay out results will be provided in Chapter V.

4.1 Circuit Simulation

This section contains the HSPICE model selection and validation, as well as design and simulation procedures for the 4-bit parallel ADC and the four-quadrant mixer. All HSPICE netlist files are referenced in Appendix A, and can be found in their respective subdirectories in the main project directory.

4.1.1 HBT Model Selection. Beginning in 1986, there have been many articles published about baseline processes for AlGaAs/GaAs HBTs [9,19,39]. Research involving both digital and high frequency applications for HBTs have been published detailing the SPICE parameters that were used to simulate the HBTs [9,25,40]. While these models do not reflect the recent gains made in the field through better processing techniques, the dc response will not noticably change with the new transistors. Therefore, the initial thrust of this research effort involved trying to reproduce Wang's results [9]. The SPICE parameters that were used are available in Table 2 with all default values included.

The first model that was acquired was a model that was developed through research work by Fellows [10]. The model was predominantly physics-based with only a small portion of the parameters derived through empirical solutions. The physics-based solutions allowed a closer look at how variations in the processing parameters and geometries affect the performance of the HBT. The model accurately predicts the performance of the AlGaAs/GaAs HBTs fabricated at Wright Laboratory. The model developed by Fellows is also presented in Table 2.

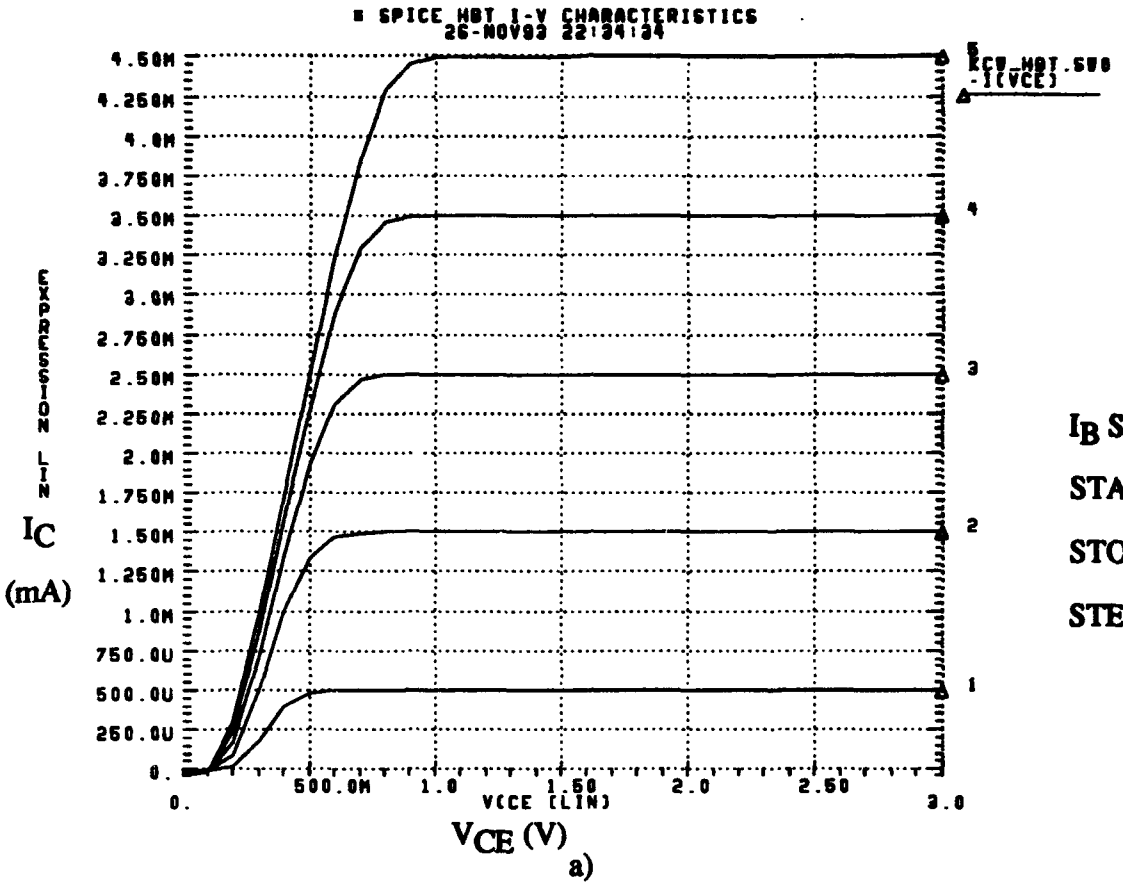
The last HSPICE model came from Rockwell [41]. This Rockwell model is specifically designed for more digital-oriented applications. The model was titled "mod6" and the model parameters are considered proprietary. A Schottky GaAs diode model was also made available which is necessary for the diode-bridge in the sample-and-hold implementation.

4.1.2 HBT Model Performance Validation. Resimulating the transistor I-V curves and the Gummel plots with the SPICE parameters given in Table 2 provided a reasonable assurance that the HSPICE circuit simulations would accurately predict operation of simulated HBT circuits. The HSPICE files that produce the dc characteristics using these HSPICE HBT models are referenced in Appendix A. The family of curves generated from HSPICE using Wang's SPICE parameters is shown in Figure 12a, and is compared to the measured data of AD2Q1, the Rockwell title for their 2.2 x 2.2 μm^2 processes, in Figure 12b.

The simulation results show several similarities and differences. The results from [9] in Figure 12b show the effect of thermal heating with increased collector-emitter voltage. As the collector current increases, the thermal heating effects create what looks like a negative conductance area on the curve. This is most dominant when the collector current increases above 3 mA. This is not represented in the HSPICE simulations due to the complexity of the model that would have to be incorporated to produce the thermal heating effects. At lower current densities, both I-V curves appear flat in the forward active regions. The small slope corresponds to an Early voltage of about 150-250 V in AD2Q1. The important aspects of the simulation show that the current values of the two plots are similar with both collector currents around 4.5 mA. An offset voltage between 0.2 V and 0.4 V was recorded for the AD2Q1 and an offset of 0.1 V can be seen from the HSPICE I-V characteristics. The voltage offset is indicated by the point to the right of the origin where the I-V curves cross from cutoff mode into saturation.

Table 2. SPICE parameters for HBT models.

Parameter	Wang [9]	Fellows [10]
BF	100	6.2943E+08
BR	1.0	0.1512
RE (Ω)	45	33.6707
RB (Ω)	150	43.2846
RC (Ω)	51	55.00
TF (ps)	3.0	0.95681
TR (ps)	350	528.7
CJE (fF)	8.6	9.8515
VJE/PE (V)	1.45	1.7018
CJC (fF)	19.0	11.19
VJC/PC (V)	1.4	1.3691
IS (10^{-25}A)	0.94	0.22354
NF	1.0	1.4832
NC	2.0	1.9698
ISC (10^{-17} A)	1800	1.0
ISE (10^{-19} A)	2390	6.2691
NE	2.0	1.8414
EG (V)	1.52	1.11
XTI	3.8	3.0
XTB	0.76	0.0
MJE	0.5	0.5
IKF	0.0	1.9E-03
XCJC	1.0	0.2053
MJC	0.33	0.5



I_C (mA)

V_{CE} (V)

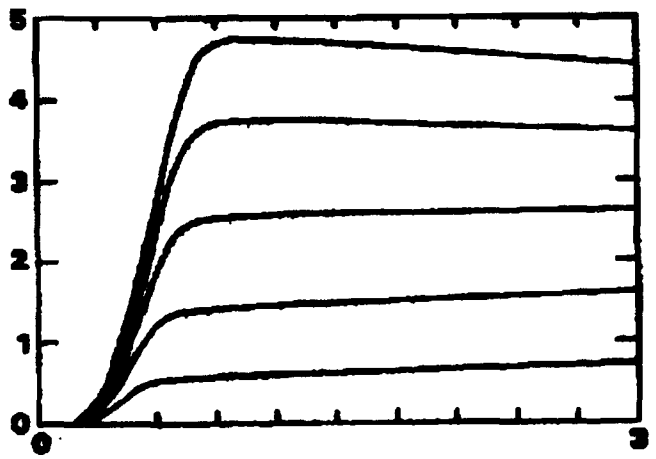
a)

I_B SWEPT:

START: 5 μA

STOP: 45 μA

STEP: 10 μA



I_C (mA)

V_{CE} (V)

b)

IB SWEPT:

START: 5 μA

STOP: 45 μA

STEP: 10 μA

Figure 12. a) HSPICE I-V curves for Wang's model and b) I-V curves for AD2Q1 [9].

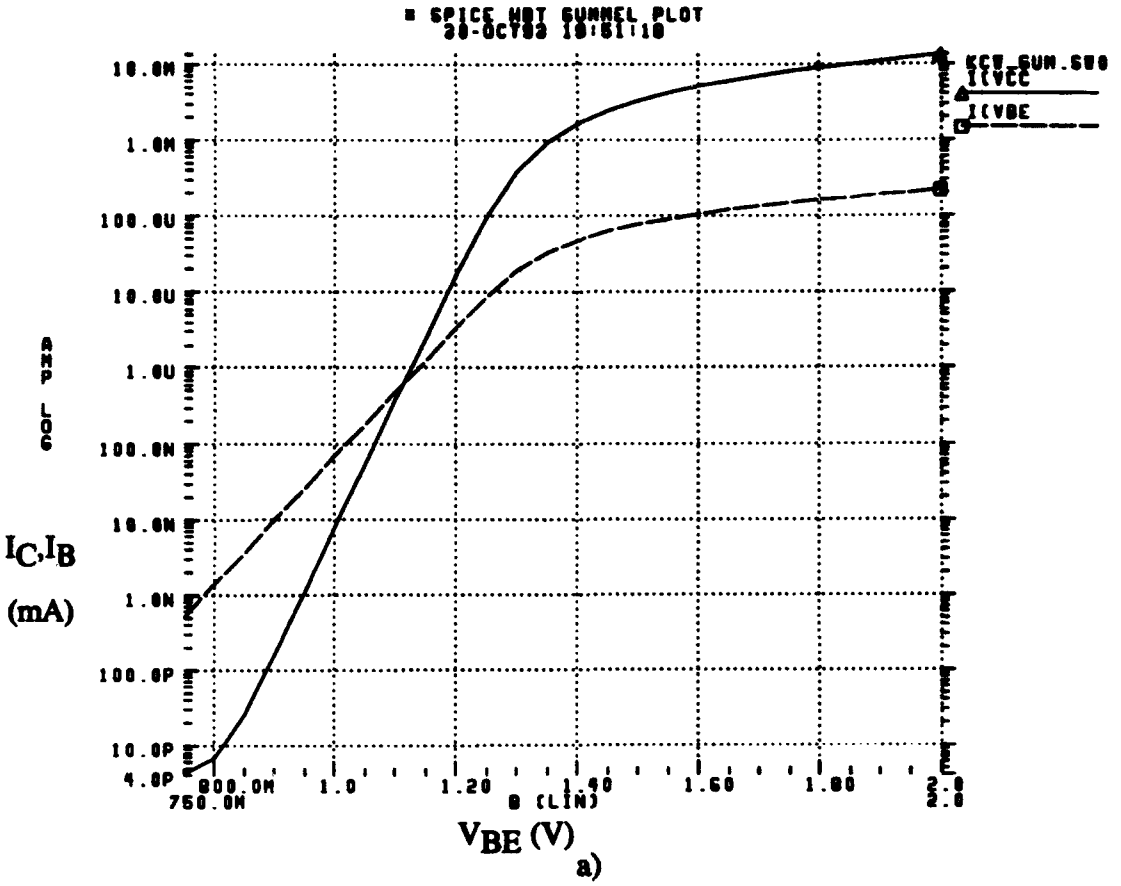
Another performance indicator is the Gummel plot which shows the base and collector currents versus the base-emitter voltage. Information can be obtained about the current gain from this chart since the dc current gain, β, can be approximated as (28).

$$\beta \cong \frac{I_c}{I_B} \tag{28}$$

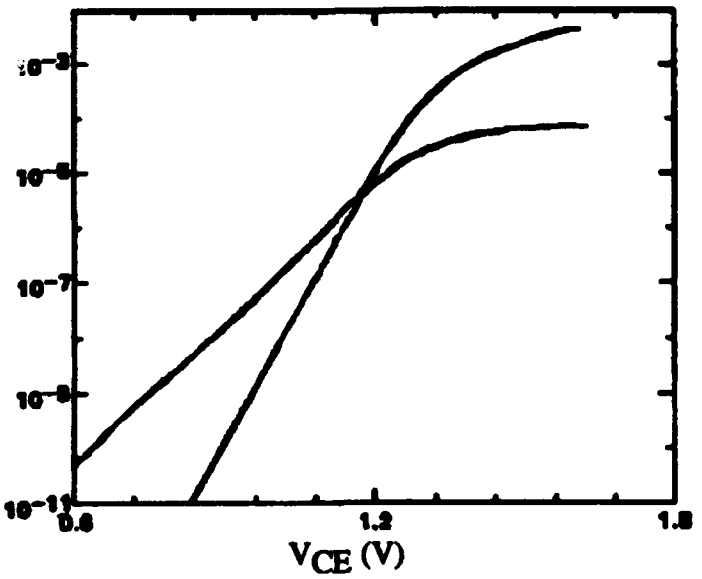
The Gummel plot for the simulated Wang model, and the Gummel plot for AD2Q1 [9] are shown in Figure 13a and 13b, respectively. Both figures show the change in the current gain over the range of the base-emitter voltage. A increasing gain is indicated as the applied voltage is increased. This is an inherent property of HBTs which is not present in homojunction BJTs. This causes transistor biasing to be a concern in circuit performance due to the a deficient current gain when driving the HBTs at smaller bias voltages. The current gain does appear constant in the region where I_C and I_B become approximately parallel.

The I-V curves for the Fellows model and the Rockwell model are shown in Figures 14 and 15, respectively. The voltage offset using the Fellows model was 290 to 300 mV and 78 to 82 mV for the Rockwell model, depending on the base current. This large difference between the offset voltages became an important factor in creating a current source from a HBT, and will be discussed in the Chapter V.

The Gummel plots for the Fellows model and the Rockwell model are shown in Figures 16 and 17, respectively. The intersection of the I_B and I_C curves for the Fellows model, which indicates the point where the current gain is one, occurs at a higher applied voltage, V_{BE}, than the respective point on the Rockwell Gummel plot. This difference in Gummel plots will explain the differences in the bias voltages for the HBT current source, and will be discussed further in the Chapter V.



a)



b)

Figure 13. a) HSPICE Gummel plot for Wang's model b) Gummel plot for AD2Q1 [9].

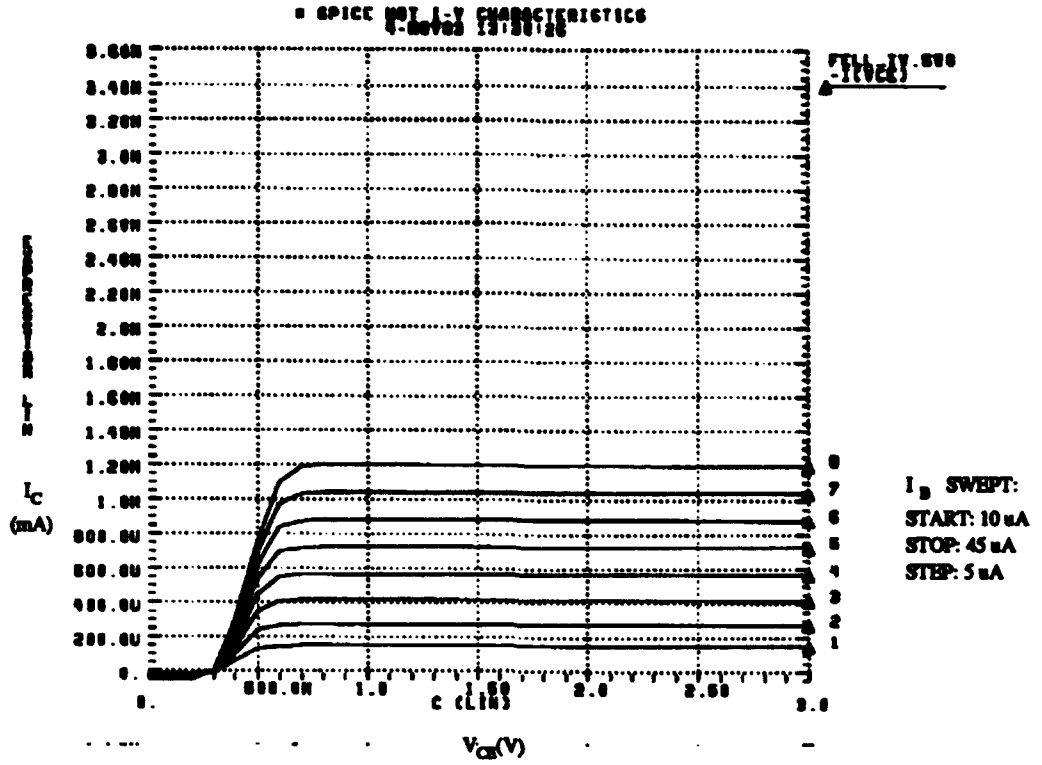


Figure 14. HSPICE I-V characteristics for Fellows HBT model.

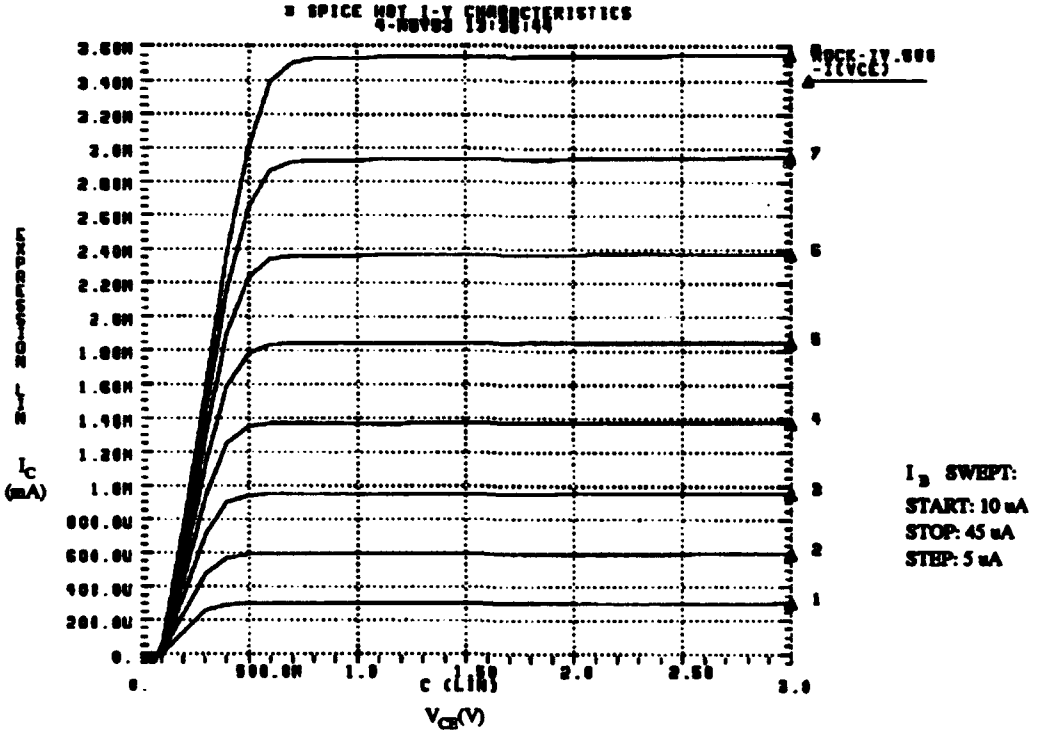


Figure 15. HSPICE I-V characteristics for Rockwell mod6 HBT model.

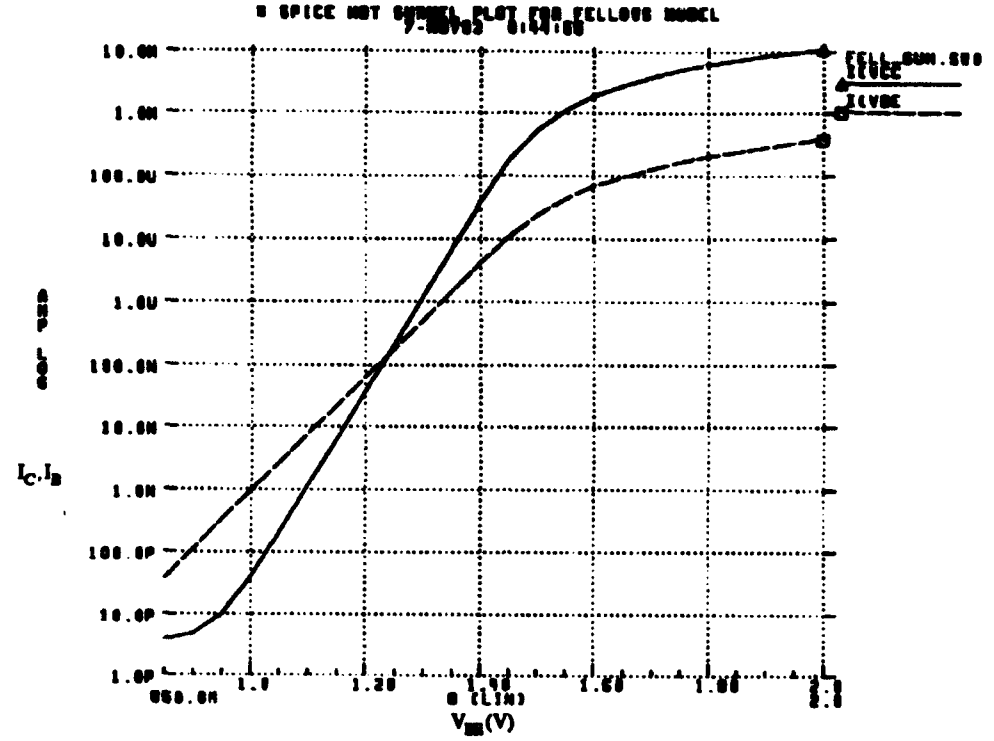


Figure 16. HSPICE Gummel plot for Fellow's HBT model.

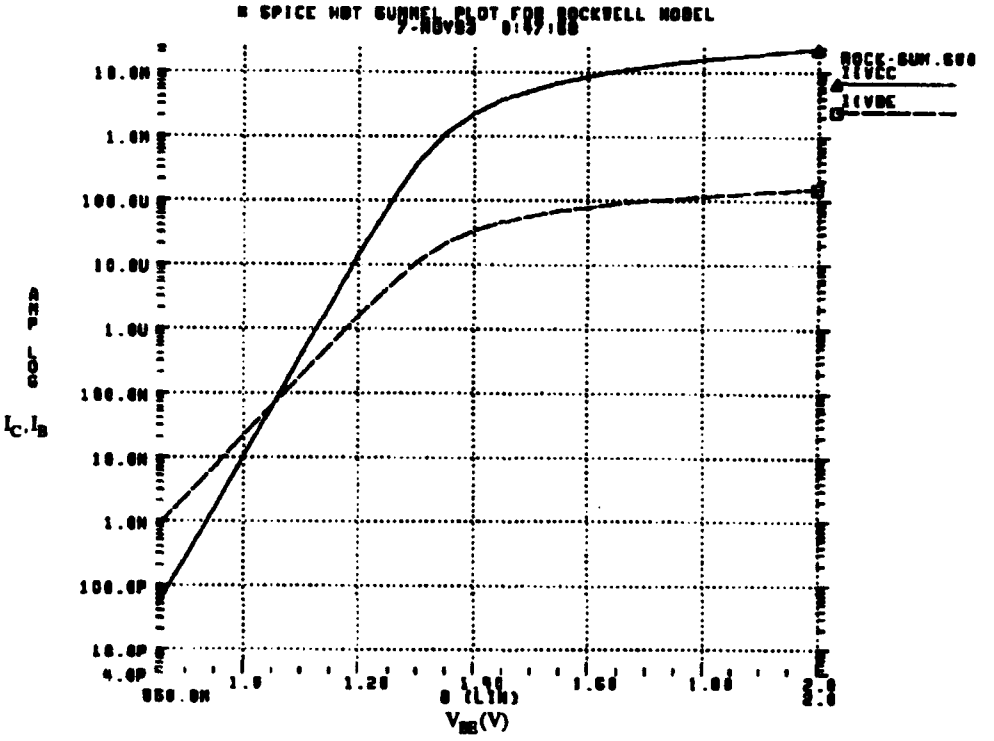


Figure 17. HSPICE Gummel plot for Rockwell mod6 HBT model.

4.1.3 Small-scale Design. The ADC can be divided into a passive stage, the reference voltage generator, and four active stages: sample-and-hold, comparators, NOR gates, and the encoding stage. The components that are implemented in this thesis are the S/H circuitry, the latched comparator, 2 and 3-input NOR gates, and four 8-input latched OR gates for the encoding stage. A simplified schematic can be seen in Figure 18.

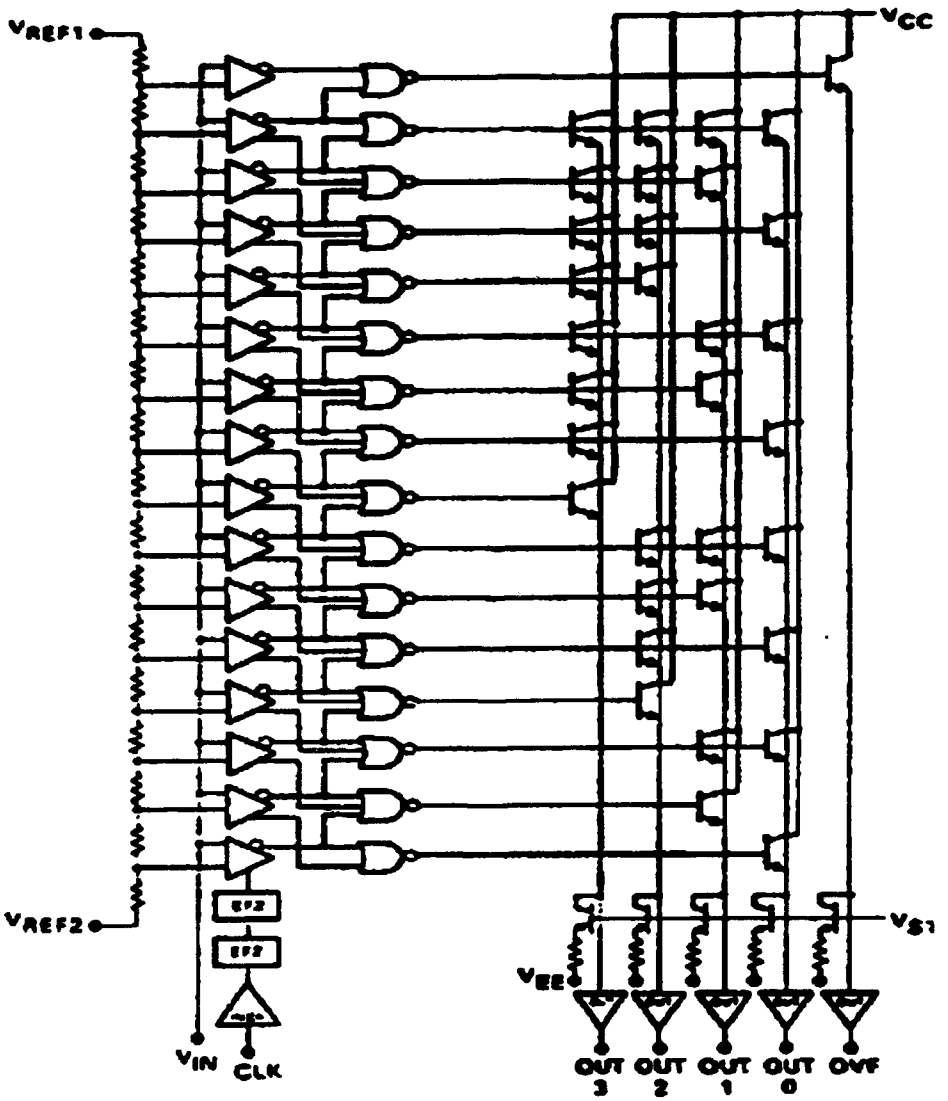


Figure 18. A simplified schematic of a 4-bit parallel ADC with three active stages [9].

4.1.3.1 Reference Voltage Generator Design. The resistive ladder is set up symmetrically so that there are quantized reference voltages for each comparator. A simplified schematic of the reference voltage generator is shown in Figure 19.

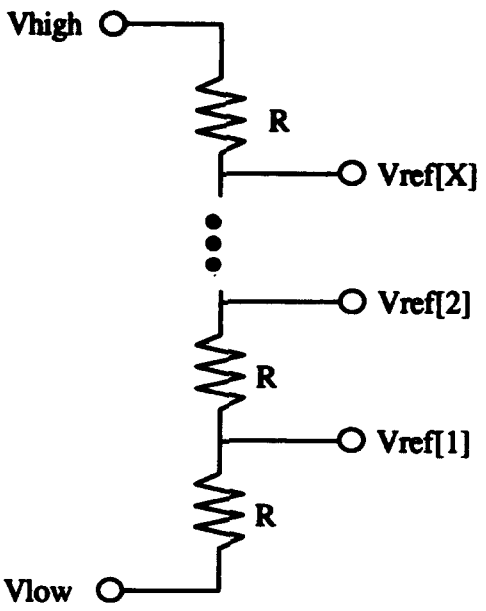


Figure 19. Simplified schematic of reference voltage generator.

The quantized voltages serve as the reference voltages, which are compared to the analog input. Vhigh is the maximum input voltage and Vlow is the minimum input voltage. The highest reference voltage is VrefX, where X represents 2^n-1 and n is the number of bits. In this thesis, a 4-bit ADC is being constructed, so only fifteen reference voltages are needed. An extra reference voltage and comparator are provided so that an overflow bit may signal when the analog voltage exceeds its maximum limit. It is crucial to have uniform resistor characteristics, because large inconsistencies in the resistivities will affect the accuracy and resolution of the ADC. Wang reported the variation in his process for Nichrome (NiCr) resistors to be less than 2 percent, so this should not pose a problem, especially if the ADC is fabricated through Rockwell [9]. The value of each resistor is independent of the analog voltage swing, but needs to be large enough that

variations in the resistivity appear insignificant to the voltage drop across a resistor. This can be seen in (29), where R_p is the parasitic resistance associated with the interconnects, and R is the value of each NiCr resistor.

$$V_{ref} = \frac{R}{17R + R_p}(V_{high} - V_{low}) \tag{29}$$

4.1.3.2 Sample-and-hold Design and Simulation. The first stage of the ADC is the sample-and-hold (S/H) circuitry, which is present to stabilize the input signal while the internal comparators and digital components have time to propagate the encoded signal to the output bits. The S/H circuitry consists of an input buffer, a clocked diode bridge circuit, impedance matching resistors, and two output buffers. The S/H implementation which appears in Figure 20 was reported by Poulton, *et. al.*, in 1988 [22].

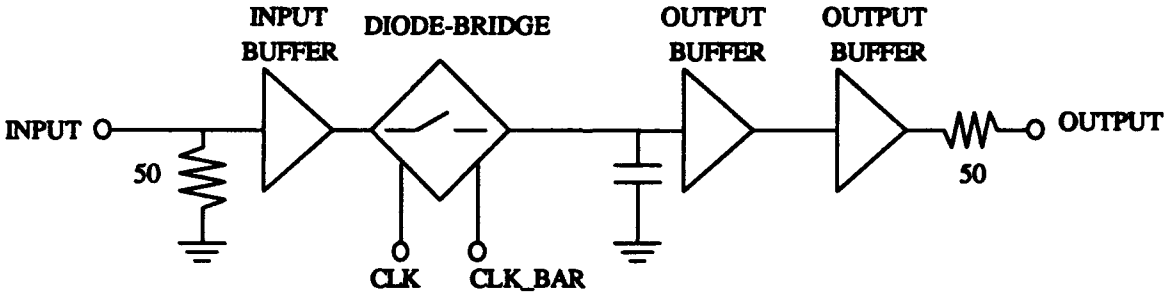


Figure 20. Block diagram of the S/H circuit.

The input buffer is a simple emitter follower. The clocked diode bridge circuit is shown in Figure 21 and is similar to a differential pair with the complementary outputs separated by the diode bridge.

The output buffer is shown in Figure 22 and consists of a unity-gain feedback buffer as the first stage and emitter follower as a second stage. The HSPICE simulation netlist for the S/H is referenced in Appendix A.

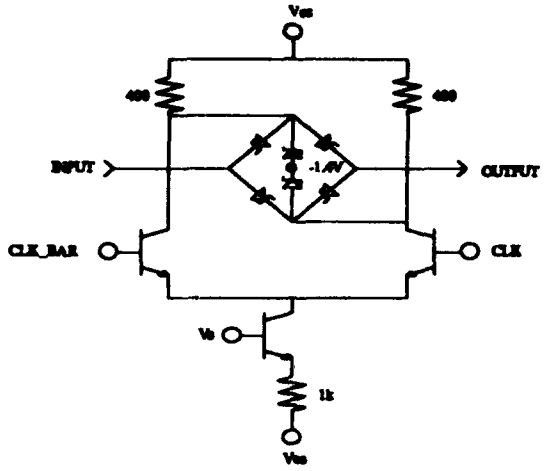


Figure 21. Clocked diode bridge circuit for S/H.

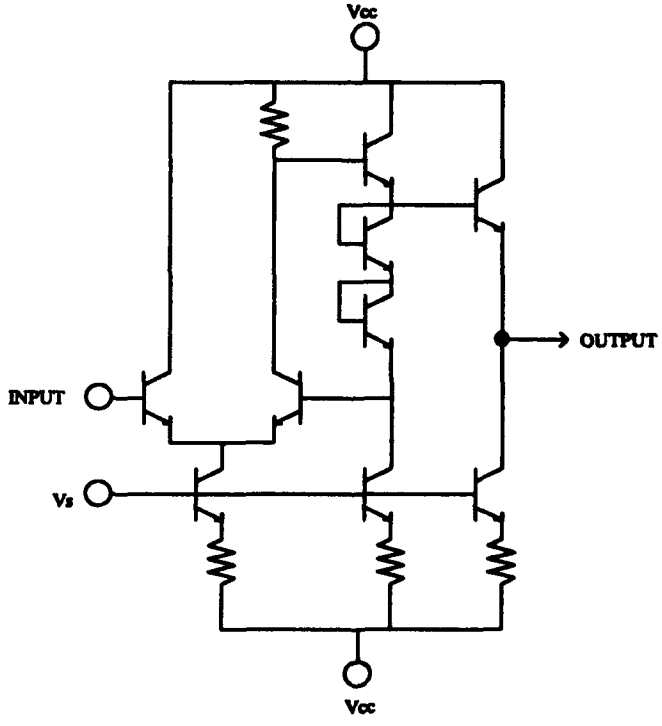


Figure 22. Circuit configuration of output buffer circuit.

4.1.3.3 Differential Pair Design and Simulation While differential pairs are not a specific stage in the ADC configuration, the importance of their performance for analog and digital applications warrants a separate section for their simulation. The differential

pair configuration can be seen in all of the digital components discussed in this thesis, as well as high-frequency components such as the mixer/multiplier.

Initial simultations were performed on a differential pair of transistors. The goal of this simulation was to determine the logic swing between the two output nodes, OUTPUT and OUT_BAR, and to be able to draw a current through the circuit using a HBT as the current source. The circuit configuration is shown in Figure 23 and the HSPICE file that was used to simulate the component is referenced in Appendix A.

The logic swing between the two output nodes must be large enough to retain a large noise margin, but a low current value is desirable to keep the power consumption low. Previous studies have shown that a resistive load of 400 Ω is an adequate size for a load with 1 mA current flowing through the circuit [9]. Ohm's law states that if there is a 1 mA current through a 400 Ω resistor, then there is a 400 mV voltage drop across the resistor. There was a concern that there could still be a residue current flowing through the opposite branch of the "on" transistor in a differential pair. A test of the current flowing through the opposite branch indicated that the current was negligible, with the residual current in the microamp range.

4.1.3.4 Comparator Design and Simulation. The second active stage of the ADC is the latched voltage comparator. This circuit can be found in two sources [9,26] and is known in more general terms as a series-gated CML comparator. The advantage of CML logic having complementary outputs can be seen from the comparator implementation, because both OUTPUT and OUT_BAR are fed to the NOR gate stage.

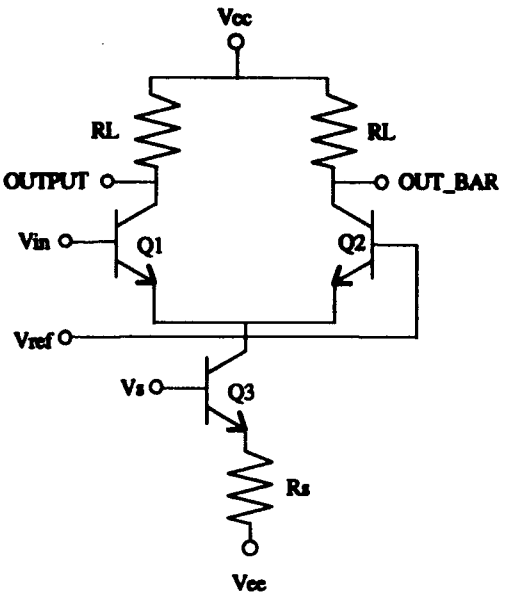


Figure 23. Circuit schematic for differential pair.

The series-gated CML configuration is useful in producing any number of logic functions depending on the complexity of the design. These gates have applications for digital circuit integration due to the flexibility of the circuit implementation. Figure 24 shows the implementation of the logical function (A+B+C)•(D+E) [42]. The input transistors at the inputs A, B, and C act like switches, which "open" the switch when the input voltage is lower then the reference voltage and "closes" the switch, allowing the current to flow through the transistor, when the input voltage is higher than the reference voltage.

The ability to get comparators that are geometrically and electronically matched is crucial for high bit accuracy and peak performance. Peak performance is indicated by a high sampling rate, which means a high-frequency clock signal, and fast rise and fall times at the output.

The clock signal in HSPICE for the comparator and all other components used rise and fall times of 50 ps. This delay time was chosen because the rise and fall times of the NOR gates were found to range between 25-50 ps, and any circuitry producing the clock

signals would probably have similar times. The power-to-ground rails to the components in the ADC, V_{cc} and V_{ee}, are set to ground and -4.5 V, respectively. The configuration of the series-gated CML comparator is shown in Figure 25.

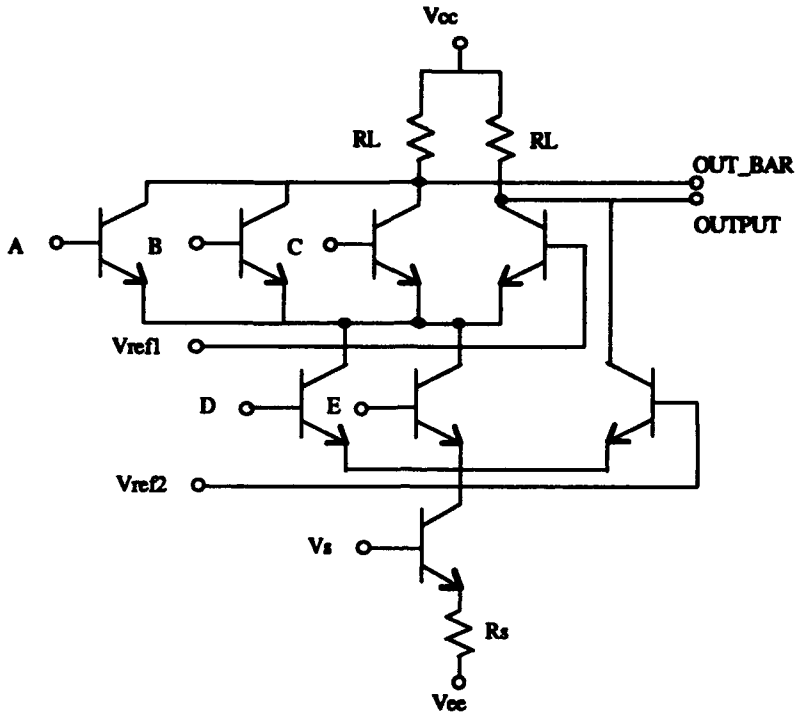


Figure 24. Series Gated Structure [(A+B+C)•(D+E)].

The inputs of the voltage comparator consist of the analog voltage (Valog), the reference voltage from the resistor ladder (Vref), and the bias voltage source (Vs) for the that serves as a current source (Q7). The series-gated comparator latch is built from three separate differential pairs. The first differential pair is Q5 and Q6 which steers the current between the right and left-hand side of the circuit. The second differential pair compares the analog input at Q1 with the reference voltage at Q2. Q5 acts as a switch, so that when the clock signal (CLK) goes high, the current is pulled down the left-hand side of the circuit. When the current is flowing through the left-hand side of the circuit, the output is following the analog input, as can be seen in the diagram in Figure 26. When the inverted

clock signal (CLK_BAR) is high, Q6 turns on and allows the right-hand side of the circuit to become active. The last differential pair, Q3 and Q4, then latches the output to either the high value (~0 V) or the low value (~-400 mV) depending on the input during the previous comparison.

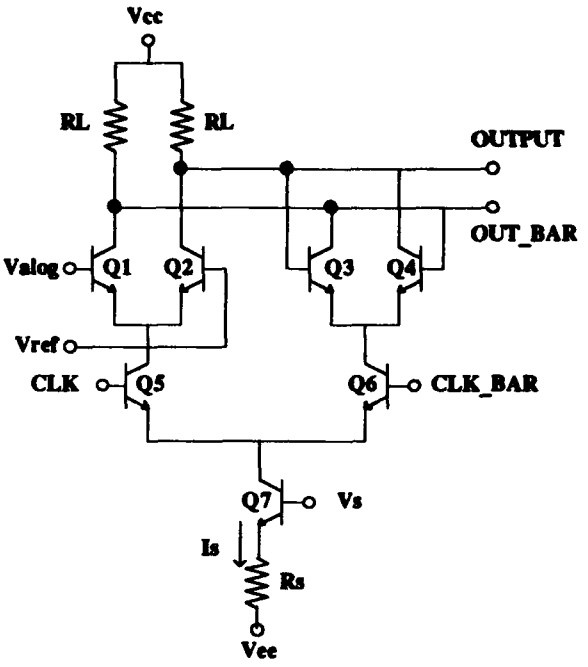


Figure 25. A CML series-gated comparator.

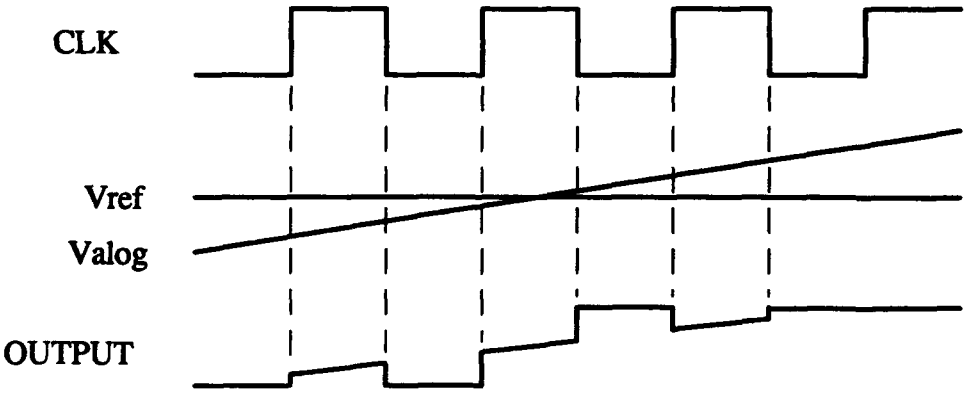


Figure 26. Operational diagram of comparator operation.

A single HBT can be used as a current source in ECL and CML circuits. The bias voltage, V_S, can be set to draw a specific amount of current from V_{CC} to V_{ee}. From a previous reference, a typical current setting is 1 mA [9]. The power dissipation is minimized by controlling the current flow through the circuit. The bias voltage, V_S, for the current source varies for different models. Table 3 depicts the necessary voltages for the Wang, Fellows, and Rockwell models to draw a 1 mA current. These voltages were found initially with R_S set to 1 kΩ. After initial design of the components with R_S=1 kΩ, it was found that it would be advantageous to set R_S=100 Ω. This would allow a lower bias supply to applied to the current source, and the resistor would take up less area. Therefore, the optimized values of V_S, with R_S=100 Ω, are also set in Table 3. The reasons why the bias voltage is greater for the Fellows model than the other models will be discussed in Chapter V.

Table 3. Bias voltage values for the current source.

Source Voltage	Wang (V)	Fellows (V)	Rockwell mod6 (V)
V_S (R_S=1000 Ω)	-2.14	-1.85	-2.12
V_S (R_S=100 Ω)	-3.0477	-2.8639	-3.0564

The voltage swing required for the clock was initially estimated from the voltage drop across the load resistor plus the turn-on voltage, V_{ceon}. This gives the voltage at the collector of Q7 in the comparator. From Figure 12, the I-V curves for Wang's model, V_{ce} needs to be at least 1 V to drive the transistor into the forward active region of operation. The voltage across the load resistor, R_L, was 400 mV, so the voltage at the collector of Q5 was estimated to be -1.4 V. In the forward active mode, the base-emitter junction must be forward biased and the base-collector junction must be reverse biased. It follows, then, that the intrinsic collector voltage must be the highest voltage, with the

intrinsic base voltage slightly lower for reverse bias conditions, and the intrinsic emitter voltage even lower than the base voltage to provide a forward bias condition at the base-emitter junction. After performing a simulation with the clock signal at -1.6 V, the emitter voltage was discovered to be -3.33 V, which was used as a gauge to drive Q5 into the cutoff mode. This voltage swing, -1.6 V for the high voltage and -3.5 V for the low voltage, was then used for the clock signal. After adjusting the voltages to prevent the base-collector junction from becoming forward bias, thus entering the reverse active mode, a -1.6 V to -3.0 V voltage swing was adopted for the clock signal.

When CLK drives Q5 into cutoff, CLK_BAR drives Q6 which turns on the latching side of the circuit. A check was made in HSPICE of the voltages at the nodes of the collector, base, and emitter of Q5 throughout the entire mode of operation. A plot was made of the voltages at the terminals of Q5, which can be found in Figure 27, and the transistor was found to be biased in the forward active mode when CLK was asserted, and in cutoff when CLK was low. This behavior indicates that Q5 and Q6 are functioning as desired.

Figure 27 shows Q5 operating in the forward active mode during the comparison stage (CLK high), and in the cutoff mode while latching (CLK low). The forward active mode occurs when the base-collector junction is reverse biased, and the base-emitter junction is forward biased. The comparator was then simulated using the circuit parameters listed in the Table 4. The results are detailed in Chapter V.

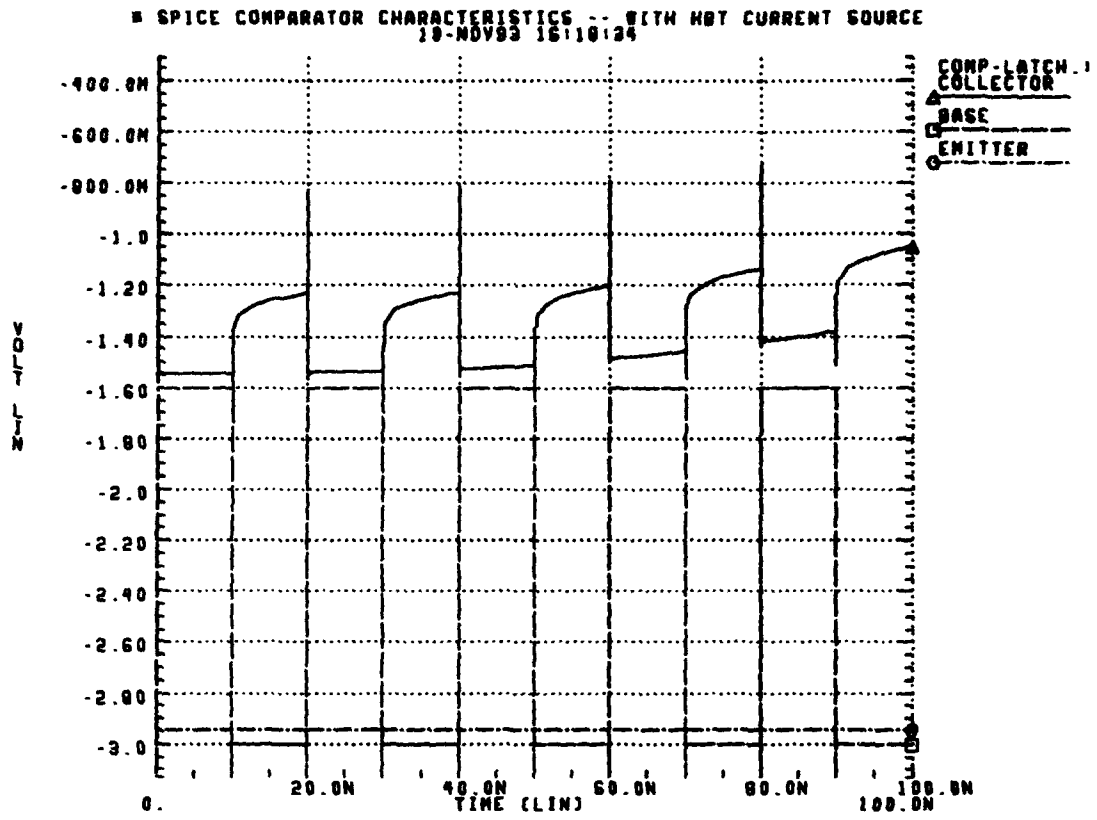


Figure 27. Terminal voltages for collector, base, and emitter of Q5 from HSPICE.

Once the series-gated comparator was simulated, the slave stage was added to the master stage to make a complete latch. This configuration allows the master portion to latch when CLK is high, and the slave portion to latch when CLK is low. This way one of the two stages must be latching for any stable clock cycle, which provides stability to the output. The HSPICE netlist for the series-gated CML comparator and the master-slave configuration of the comparator, along with its subcircuit netlists, are referenced in Appendix A. The circuit implementation of the master-slave configuration is shown in Figure 28 [43], and the diagram for the input, output, and clock signals of the master-slave comparator is shown in Figure 29. The predicted results will be compared to the actual results in Chapter V.

Table 4. Comparator input parameters.

Parameter	Value
CLK(inverted CLK_BAR)	-1.6 to -3.0 V at 1 GHz
V_{cc}	0 V
V_{ee}	-4.5 V
V_{alog}	Linear rise: -0.4 V to 0 V in 20 ns
V_{ref}	-0.2 V
Vs	Dependent on HBT model (see Table 3)
R_L	400 Ω
Rs	1 kΩ

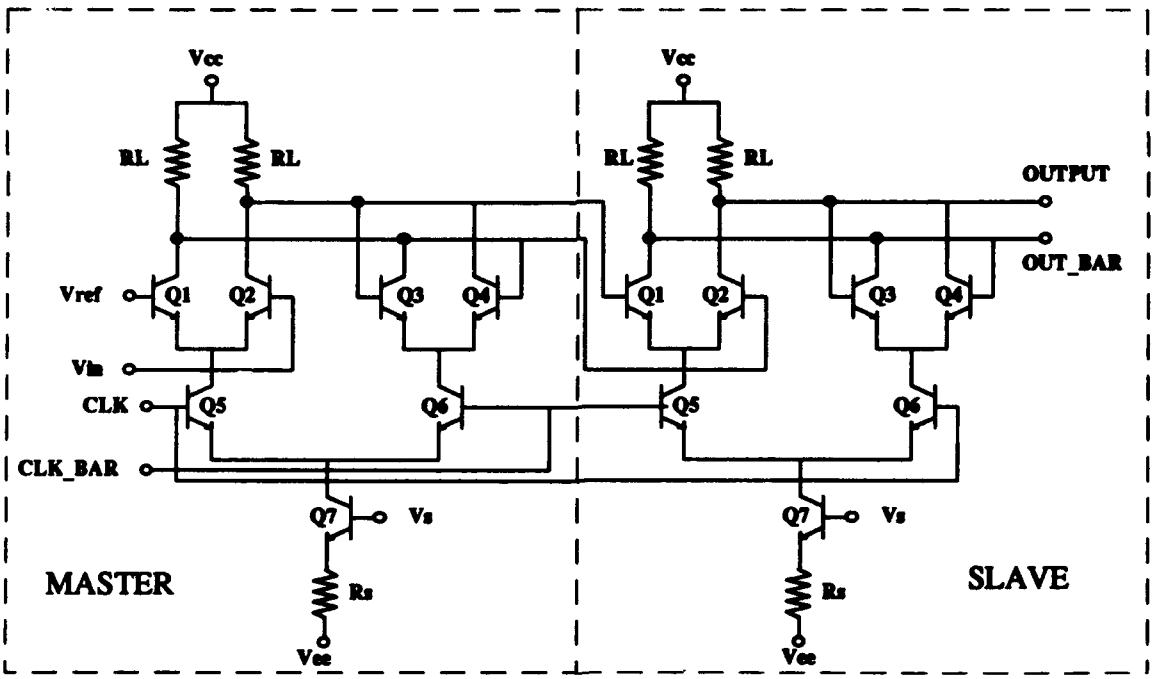


Figure 28. Master-slave configuration for series-gated CML comparator.

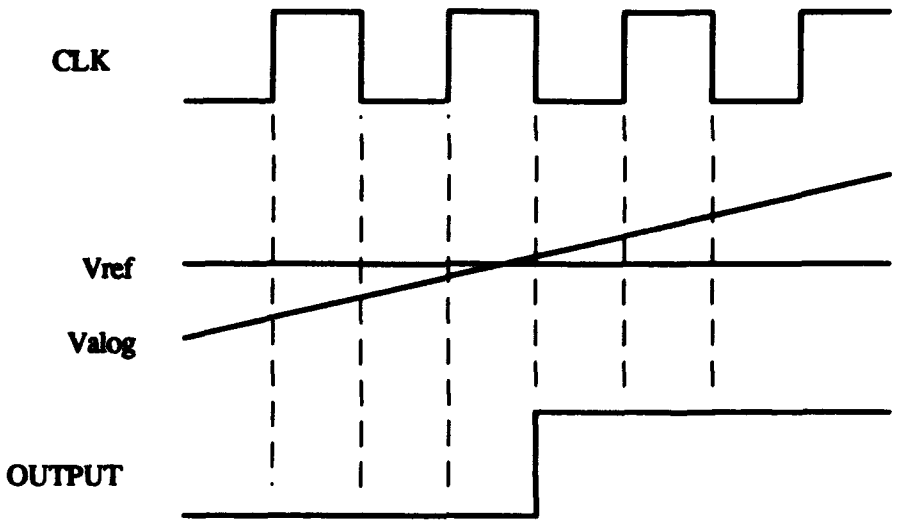


Figure 29. Operational diagram for master-slave comparator.

4.1.3.5 NOR/OR Gate Design and Simulation. The NOR/OR gate is a digital circuit implemented using CML. The 2-input NOR/OR gate consists of a differential pair where the left side of the pair has two transistors in parallel with the inputs connected to the bases of Q1 and Q2, as seen in Figure 30. The reference voltage is placed at -0.2 V, which is midrange of the output logic swing. The resistive loads between the output nodes, OUTPUT and OUT_BAR, and V_{CC} are again placed at 400 Ω. Setting the current source to 1 mA requires the bias voltage appropriate for the individual HBT, as listed in Table 3, with the 1 kΩ resistor between the source transistor and Vee. The logic swing seen at the output is approximately 400 mV. In this application, even though complementary outputs are available on the NOR gate, only the NOR output is needed. The netlist used to simulate the 2-input NOR/OR gate is referenced in Appendix A. The 3-input NOR/OR gate is produced in the same way as the 2-input gate, but three transistors are placed in parallel instead of two. The three transistors are labeled Q1, Q2, and Q3. A schematic of a typical CML 3-input NOR/OR gate is shown in Figure 31. The HSPICE netlist for the 3-input CML NOR/OR gate is referenced in Appendix A.

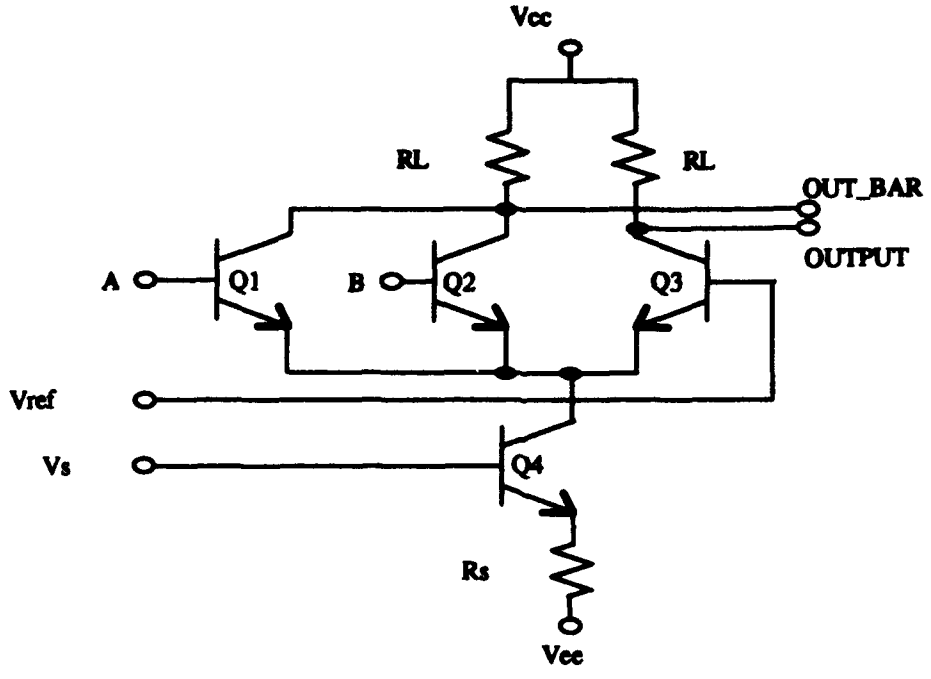


Figure 30. A CML 2-input NOR/OR gate.

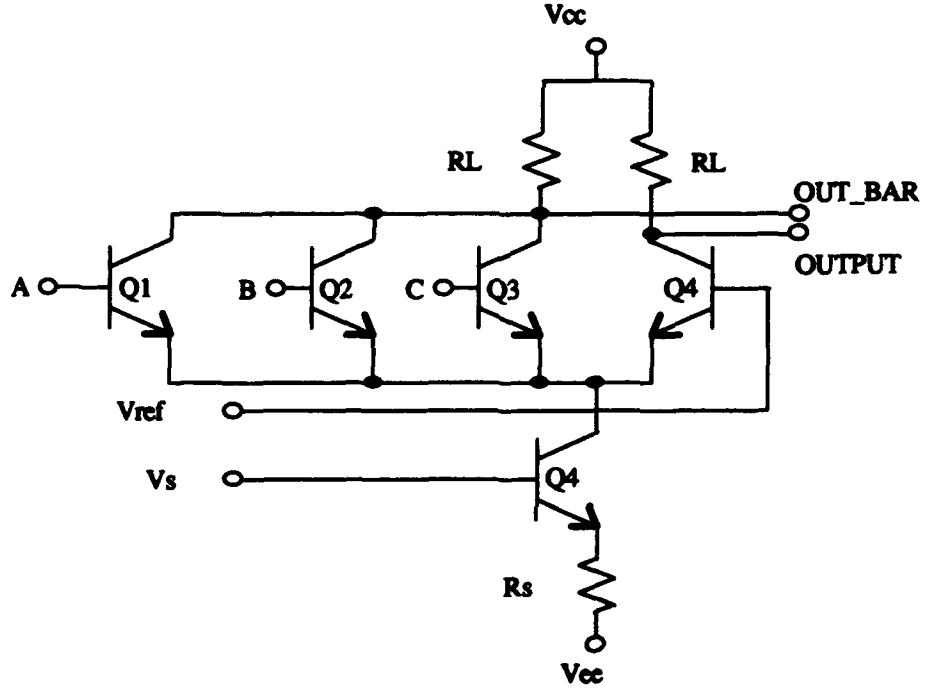


Figure 31. A CML 3-input NOR/OR gate.

4.1.3.6 8-input OR Gate. The final component that provides the necessary encoding and latching at the output is the 8-input latched OR gate. The original plan was

to create the typical NOR/OR gate and then develop an output latch that captures the digital data at the output. However, if the series-gated comparator is modified so that seven other transistors, Q9-Q15, with the bases connected to the inputs, are placed in parallel with the input transistor, a latched 8-input NOR/OR gate can be achieved. The general configuration of the series-gated OR gate is shown in Figure 32. The reference voltage at the base of Q2 would be set at -0.2 V, which is the center voltage of the output swing of the NOR gates. The latched 8-input OR gate is then followed by a series-gated comparator as the slave stage, similar to the master-slave configuration of the comparator. The netlist for the 8-input OR gate and the netlist for master-slave configuration of the OR gate are referenced in Appendix A.

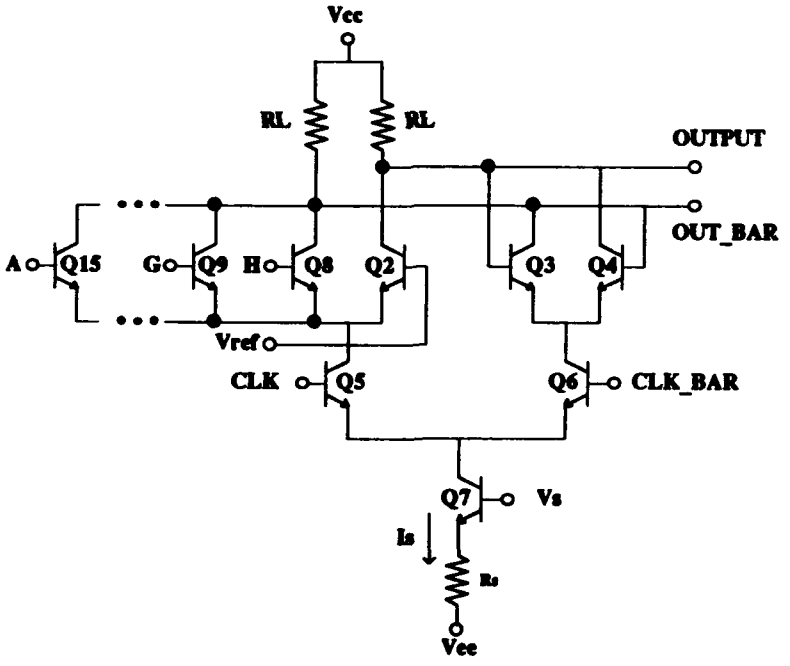


Figure 32. An 8-input series-gated CML OR gate.

4.1.4 Design of High-frequency Mixer. The mixer is used for high-frequency conversion from radio frequencies to intermediate frequencies that mixed-signal circuits, such as ADCs, can accept. The mixer implementation takes a known local oscillator (LO)

and a radio-frequency (RF) signal and converts it to a intermediate frequency (IF) as shown in Figure 2. The HSPICE netlists for the mixer are contained in Appendix B. Simulation results are located in Chapter V.

4.1.4.1 Gilbert Multiplier Cell. The basic configuration of a mixer can be based on a Gilbert multiplier cell reported in 1960s [44]. The Gilbert cell allows four-quadrant operation and is shown in Figure 33. Four-quadrant operation means that the RF input voltage can be both positive and negative, as opposed to two-quadrant operation where the RF input voltage must be positive. This circuitry is largely based on ECL as indicated by the differential pairs. Therefore, the circuit will be built employing the knowledge gained from the design of the CML components of the ADC.

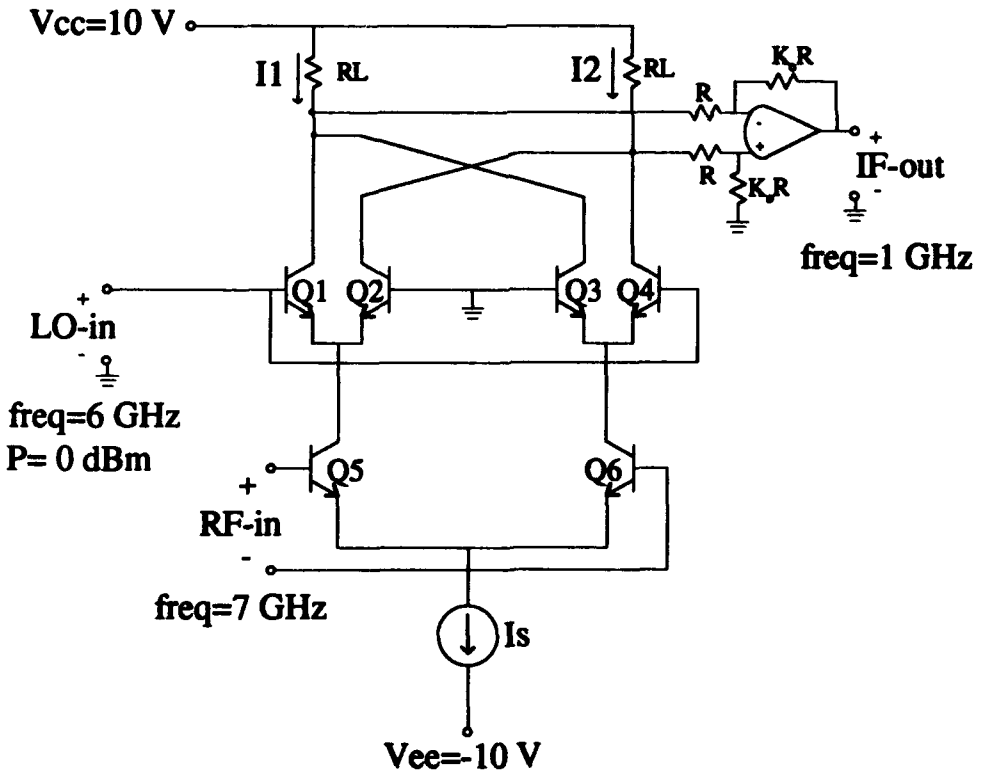


Figure 33. Gilbert multiplier cell.

A standard power setting of 0 dBm for the LO input was used in a reference by Osafune [38]. The unit dBm is the power level relative to 1 mW, so the voltage amplitude for the LO input is 0.316 mV according to (30) below.

$$P = \frac{1}{2} \cdot \frac{V_{max}^2}{R} \tag{30}$$

The value of R was standardized to 50 Ω and was confirmed by finding the Z parameters of the cell at the LO input with the RF input set to zero. Z_{11} was found to be approximately 50 Ω from 10 MHz to 10 GHz, which is the typical frequency range for the mixer. The output impedance, which was simulated by finding Z_{22}, was also found to be approximately 50 Ω over the same frequency range. When the LO input was set to zero and the Z parameters were measured at the RF input, the same results were obtained with 50 Ω impedances over the same frequency range. This standardization allows easy calculation of the power gain and isolation measurements within HSPICE. S parameters, which measure the reflected and transmitted signals at the input and port to the circuit, were also used to calculate the gain of the Gilbert cell. The results of the gain simulations will be presented in Chapter V.

The output logic swing was detemined by the load resistors, R_L, which were set at 400 Ω, the standard seen in a few mixer references [38,45]. The output of the Gilbert cell is followed by an operational amplifier (opamp). The opamp was implemented as an ideal amplifier in HSPICE with a gain of 5. The resistors leading into the opamp, R, are set to 1 kΩ, which is high enough to prevent distortion that is present at low resistor values. The value of K_O was found to be 4 using optimization techniques. When the feedback resistor, $K_O R$, was set to 4 kΩ, a minimum amount of distortion was obtained, for a reasonably high gain. The results of the mixer will also be presented in Chapter V. An opamp designed using HBT technology was not observed in the literature review, but may be implementable in the future.

While the CML components had a current of 1 mA from the current source, the reference articles indicate that a larger current source is needed to achieve operation. A report by Wholey, *et. al.*, in 1989, reveals a 12 mA current output with 5 V voltage supply as Vcc [45]. The authors also developed a 50 mA current output with a 10 V voltage supply. This implementation used 1.8 mA sources for the 5 V supply and 4.3 mA for the 10 V supply. Since literature review did not reveal any voltage supplies for HBT implemented circuits, the 10 V supply was chosen for the HBT implementation due to its ability to sink larger currents for power applications.

The amplitude of the RF input was varied from -40 dBm to 0 dBm [38]. This corresponds to voltage amplitudes of 3.16 mV and 316 mV, respectively. In order to permit the LO and RF inputs to become this large, an input stage that functions as an inverse hyperbolic tangent characteristic must be added as a predistortion circuit. The reasons for this addition will be discussed in the next section.

4.1.4.2 Input Circuitry. The Gilbert cell shown in Figure 33 has a limitation factor with the input range. The limitation is that the LO and the RF input voltage amplitudes must be small to approximate a linear output function. The hyperbolic tangent function present in the differential current between I_1 and I_2 is shown in (31) [46].

$$\Delta I = K\left[\tanh(\frac{V_{RF}}{2V_t})\cdot\tanh(\frac{V_{LO}}{2V_t})\right] \tag{31}$$

K is a coefficient dependent on the value of the current source. An inverse hyperbolic tangent characteristic at the input cancels the hyperbolic tangent characteristic present in the Gilbert cell and allows a broader amplitude range for the LO and RF input. The circuitry that provides the predistortion characteristic is shown in Figure 34. The

predistortion circuit was added to both inputs to increase the amplitude range for the input signals. The netlist for the Gilbert cell with this input circuitry is contained in Appendix B.

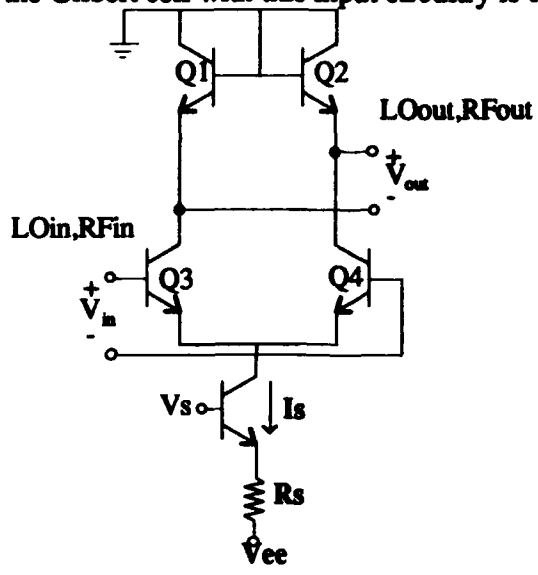
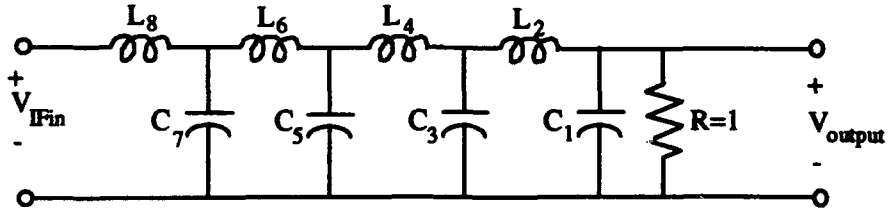


Figure 34. Inverse tangent hyperbolic characteristic circuit.

4.1.4.3 Passive Output Filter. An output filter was designed to filter out the higher-frequency components of the output signal. Because both MIM capacitors and inductors were available for fabrication at Wright Laboratory, a passive filter was chosen as the best candidate. An 8-pole, 1-dB ripple, Chebyshev low-pass filter using single-resistance-terminated lossless ladder was implemented and is shown in Figure 35 [47]. The specifications for the filter are -78.5 dB at 6 GHz, and -91 dB at 7 GHz, where the greatest distortion existed, with only a ±1 dB attenuation below 3 GHz. The filter is designed for a voltage input from the opamp of the Gilbert cell.



C_1=57 pF C_3=57 pF C_5=114 pF C_7=111 pF

L_2=78.5 pH L_4=90 pH L_6=90.5 pH L_8=72.8 pH

Figure 35. Low-pass passive 1 dB ripple Chebyshev filter.

4.2 Circuit Layout

This section shows the steps involved in the layout of the small and large-scale circuits for this thesis effort. The layout involves resistors, as well as HBTs. The Wright Laboratory (WL) process allows nichrome (NiCr) and collector epilayer (epi) resistors to be fabricated. The Rockwell process allows NiCr and tungsten-silicon-nitride (WSiN) resistors to be fabricated. Since resistors of 400 Ω or less will be fabricated, the NiCr resistor will be used to allow better control over sheet resistivity. The sheet resistivities for the WL HBT process are 25 Ω/□ for the NiCr resistors and 300 Ω/□ for the epi resistors. The sheet resistivities for the Rockwell HBT process are 50 Ω/□ for the NiCr resistors and 500 Ω/□ for the WSiN resistors. The layers for the NiCr resistors are present in the Rockwell HBT technology file, but layers were added to the WL technology file to implement the NiCr resistors. A layout of the NiCr resistor is shown in Figure 36. The names of all Magic components are referenced in Appendix C.

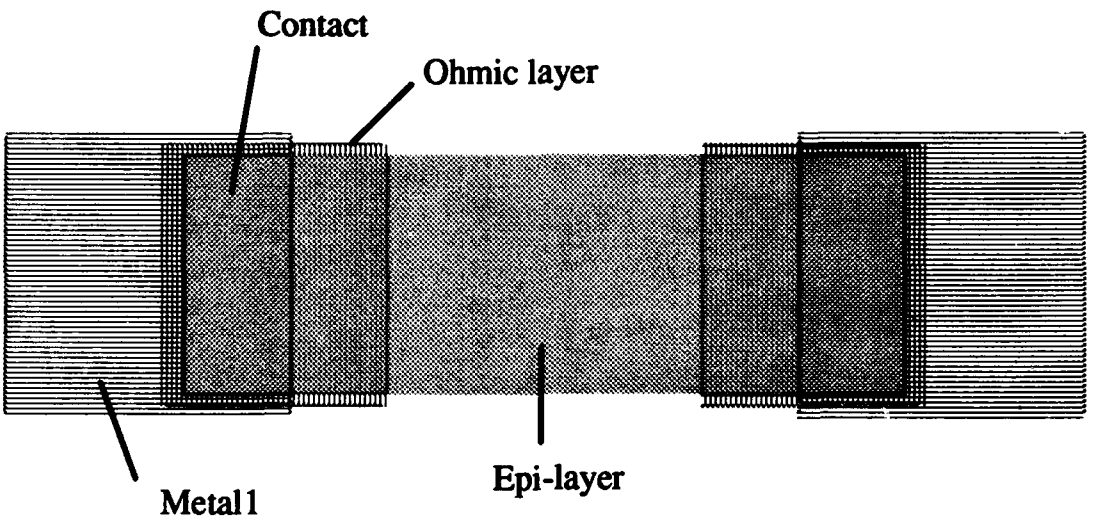


Figure 36. Nichrome resistor for WL technology file.

4.2.1 Magic Layout Editor

The Magic technology file is the key to extracting transistors and parasitics. The technology file is not a program written in high-level language, but a tool that defines parameters for a specific technology, such as HBT technology. It defines the layers and planes within a layout that are electrically active, the types of contacts, design rule checking, and extraction rules. The type of technology can be defined by the designer and implemented using specific guidelines.

The majority of the layout has been completed in Magic. A limitation in Magic that was overcome was the inability to extract HBTs into netlists and convert the netlists into SPICE subcircuits. The netlist is produced so that a layout versus schematic (LVS) check can be performed. Some vendors will not fabricate circuits unless the LVS check has been done. The Magic technology file and the conversion program *ext2spice* can be used for transistor and parasitic capacitance extraction. The parasitic resistances can be extracted using the technology file and *ext2sim*.

The *fet* statement allows active devices to be found such as the p-channel FET (*pfet*), n-channel FET (*nfet*), enhancement p-channel FET (*epfet*), and enhancement n-channel FET (*enfet*). An example of the fet extraction line is shown as:

fet pfet pdiff,pdc 2 pfet Vdd! 0 0

The line extracts any *pfet* tile that is surrounded by two terminals consisting of *pdiff* or *pdc*. The model name that propagates through to the simulation tool is *pfet*. The substrate is always connected to *Vdd!*. The two zeros indicate that gate-channel and gate-substrate capacitance is negligible. The most current release of the CMOS technology file (*scmos.tech26*) also shows a way to extract p-n diodes, which are then connected in the schematic to form a BJT. An example of the BJT extraction line is shown as:

fet emit,emc pbase,pbc 1 nhbt Error! 0 0

The line extracts any *emit* or *emc* tile that is surrounded by one terminal consisting of *pbase* or *pbc*. The model name that propagates through is *nhbt*. The substrate is always connected to an *Error!* layer, which can be altered in the extracted netlist before simulation. More information can be found in the *extract* section of the technology file manual [48].

The new transistor extraction statement draws on the FET and diode extraction statements, but allows the direct extraction of HBTs and appears as:

fet emit,emc pbase,pbc 1 nhbt Error! collector 0 0

The layout of the HBT in magic is similar to the layers in Figure 37. The extractor looks for a layer called *emit* or *emc* and then looks for one terminal consisting of the layer *pbase* or *pbc*. If a layer *collector* is beneath the *emit* layer, the extractor will connect the substrate to the collector, else it will connect the substrate to an error layer. This configuration is carried into the extraction software as a data structure listing the emitter as the gate, the base as the source, and the collector as the substrate connection. The technology file that contains the extraction section for HBT technology is contained in Appendix D.

Magic then stores the information on each transistor in a file with the *.ext* extension, which lists the extracted nodes, their lumped capacitances and resistances, and the extracted transistors with their respective terminals and location in the Magic layout. A copy of a sample *.ext* netlist is shown in Figure 38. The Magic extractor formats the FET description in the order of *fet* identifier, model name, four position coordinates within Magic layout, area of transistor, perimeter of transistor, substrate connection layer, gate terminal, gate attributes, source terminal, and source attributes.

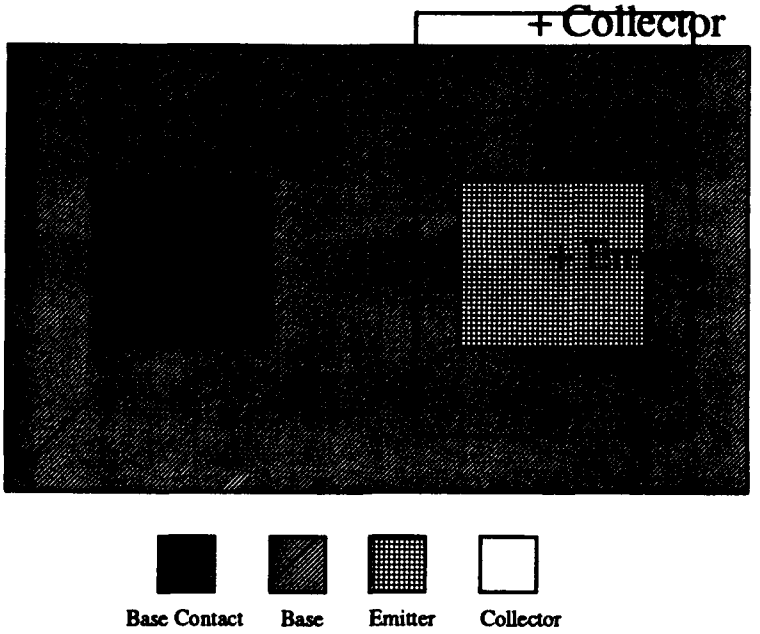


Figure 37. The configuration for an HBT in Magic.

```
timestamp 751309017
version 5.0
tech hbt
scale 1000 1000 100
resistclasses 50000 25300 50 20
node "GND!" 1 38 -13 -96 m1 0 0 0 0 1578 292 0 0
node "Vs!" 0 13 -13 -67 m1 0 0 0 0 539 120 0 0
node "C2" 1 34 -17 49 m1 0 0 0 0 1428 318 0 0
equiv "C2" "C1"
equiv "C2" "Vdd!"
node "E3" 0 0 58 -64 em 0 0 0 0 0 0 0 0
node "E2" 0 0 80 19 em 0 0 0 0
node "B1" 0 0 -6 12 pb 0 0 0 0 0 0 0 0
node "6_126_78#" 63 0 63 39 dum 0 0 40 28 0 0 0 0
node "6_2_78#" 63 0 1 39 dum 0 0 40 28 0 0 0 0
node "Vs!" 0 13 -13 -67 m1 0 0 0 0 539 120 0 0
cap "Vref" "C3" 3
fet nhbt 58 -64 59 -63 16 16 "C3" "E3" 0 0 "B3" 10 0
fet nhbt 80 19 81 20 16 16 "C2" "E2" 0 0 "B2" 10 0
fet nhbt 17 19 18 20 20 18 "C2" "E1" 0 0 "B1" 12 0
```

Figure 38. A sample *.ext* netlist.

Ext2spice is the program that converts the information within the *.ext* netlist into a separate netlist with the extension name *.spice*. This program is usually called from within the UNIX C-shell script, *ext2hsp*, which cleans up the *.spice* netlist produced in *ext2spice*. The *.sp* netlist produced from the *ext2hsp* program is used as a subcomponent for HSPICE simulations. The code within *ext2spice* was altered so that it could identify the name of the transistor being extracted, and use a different format for the *.spice* netlist used for simulations. The only subroutine that was altered was the *fetVisit* routine, which is listed in Appendix E. If the routine identifies *fet_type*, a pointer to a data structure, as being *nhbt*, it prints the model name and the transistor terminals in the HSPICE BJT format to the *.spice* netlist for simulation. If the typical FETs are listed in *fet_type*, the routine follows the HSPICE FET format. The code for producing the HSPICE BJT format prints the collector (*subsNode*), base (*sNode*), emitter (*gNode*), and the transistor model name (*fet_type*).

Resistance extraction is crucial to HBT extraction, because the CML circuits depend on nichrome resistors to determine the output logic swing. The resistance extraction involves different external software than the technique previously described for extracting HBTs. A flow diagram that details the differences in the two techniques is shown in Figure 39.

For resistance extraction, the Magic extractor uses the *:extract* command to create a *.ext* file, which is the same as the transistor extraction technique described above. The *ext2sim* program then translates the information in the *.ext* file into a *.sim* file, *.nodes* file, and a *.al* file. After reentering Magic, the :extresist command uses the *.sim*, *.nodes*, and *.al* files to extract the resistances to a .res.*ext* file. The .res.*ext* and *.ext* netlists are then concatenated to form a netlist that contains transistors, capacitances, and resistances. This file can then be translated into an HSPICE netlist using *ext2hsp*. The results of the resistance extraction are presented in Chapter V.

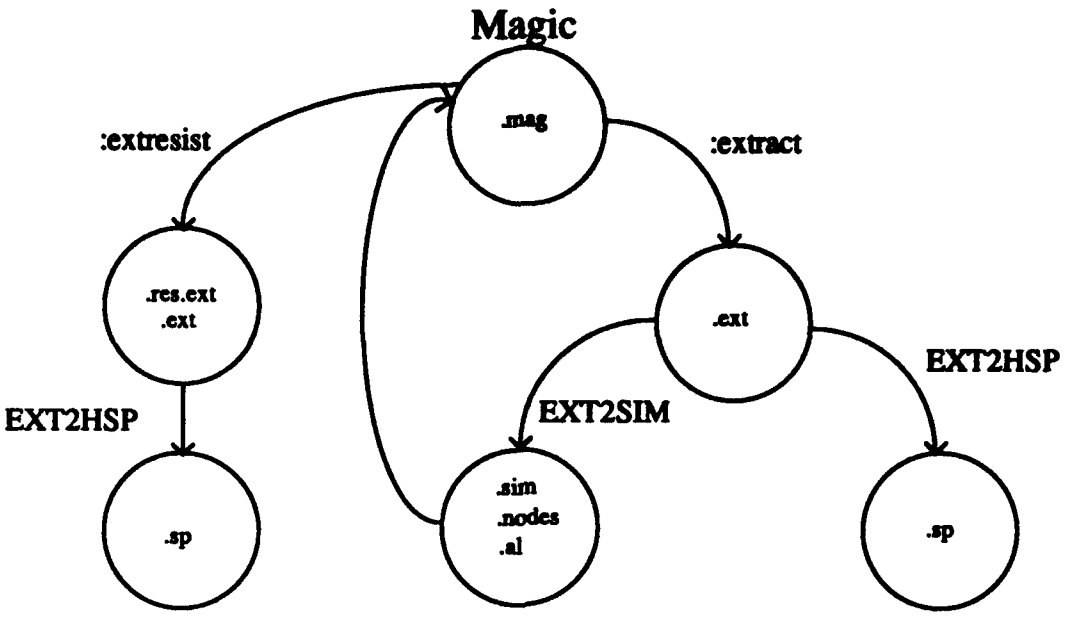


Figure 39. Flow diagram for HBT and resistance extraction in Magic.

4.2.2 DW2000 Layout Editor. For the Wright Laboratory (WL) layout, the Magic HBT technology file from Rockwell was altered to try to meet the conservative design rules used by WL in their device research. The design rules that were initiated in the technology file are shown in Appendix D along with the WL HBT technology file.

The first component that was implemented was a dummy transistor which fit the geometries of the WL HBT. Since this transistor had been developed for microwave power applications, the transistor is large. The 1-finger, 1-dot, 3 μm geometry was chosen for the ADC application and is seen in Figure 40 [49]. Since the emitter is circular, and both the emitter bridge and the collector mesa contain non-Manhattan geometries, a dummy transistor will appear in the Magic file until it can be replaced with the original in the DW2000 layout editor. The dummy transistor is shown in Figure 41, and the Magic layout is referenced in Appendix C. The emitter, emitter bridge, base mesa, and collector epi-layer are labeled, and the dummy transistor dimensions are similar to the WL HBT, but are not shown for proprietary reasons.

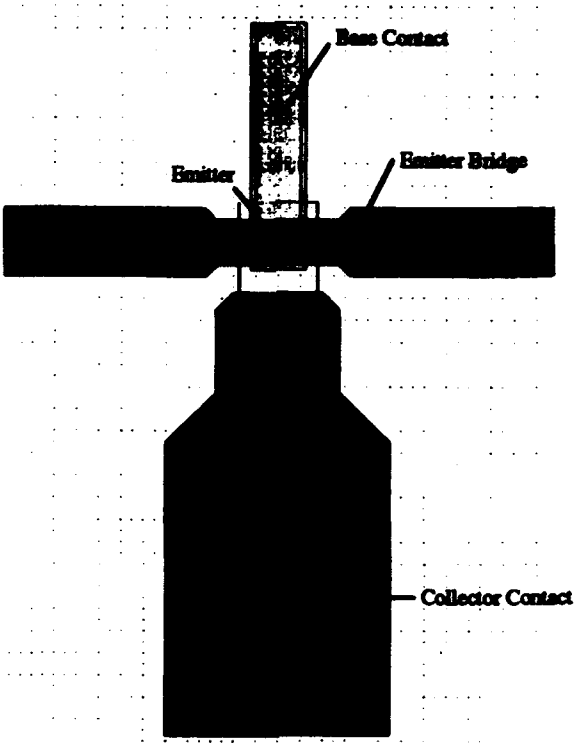


Figure 40. Wright Laboratory HBT [49].

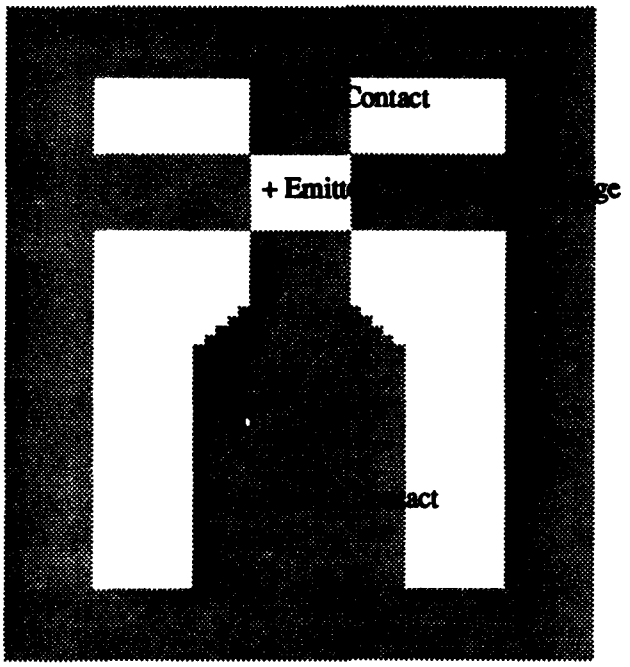


Figure 41. Layout of dummy transistor in Magic.

The next Magic component that was the basis for CML circuits was the differential pair. The differential pair was used in the construction of all the subcircuits which include the series gated CML comparator, 2 and 3-input CML NOR/OR gates, and 8-input latched OR gates. The master-slave configurations for the comparator and OR gate were developed using the series-gated comparator and the 8-input latched OR gate. The top-level component was the ADC. The ADC was implemented in Magic without a sample-and-hold due to time constraints.

4.3 Summary

The simulated I-V characteristics and Gummel plots using Wang's model closely follow the measured data from AD2Q1. The simulations should predict accurate transistor performance in integrated circuits using Wang's SPICE parameters.

The CML components of the 4-bit parallel ADC were implemented with 400 Ω load resistors and 1 mA current sources, which created a 400 mV output logic swing. HSPICE netlists for the ADC were created using HBT models from Wang, Fellows, and Rockwell [9,10,41]. The implementation of the 8-input OR gate as a latched component shows the versatility of the CML logic family. The four-quadrant double-balanced mixer based on the Gilbert cell multiplier was then implemented using the Wright Laboratory HBT. The mixer included input circuitry which broadened the voltage range of the RF input, and output of the mixer was fed to a low-pass Butterworth filter.

The layout of the ADC components were accomplished twice in Magic, first using design rules for Wright Laboratory, and again using Rockwell design rules. The layout for the mixer was not completed due to time constraints.

The technique for extracting FETs and resistors using the SCMOS technology file was altered to extract HBTs. The programs *ext2spice* and *ext2sim* were changed to create HSPICE netlists for either the BJT format or FET format. This will allow HBT layouts to be extracted and validated for proper connectivity.

V. Results

This chapter shows performance characteristics for the individual components: sample-and-hold, comparators, 2 and 3-input NOR gate, 8-input OR gate, voltage quantizers containing the comparators and NOR/OR gates, and high-frequency mixer. It also contains the changes to the code in *ext2spice* and *ext2sim* to enable Magic to extract HBTs and to create HSPICE netlists with resistive and capacitive parasitics.

5.1 Sample-and-Hold Simulations

The performance parameters for the sample-and-hold (S/H) circuitry are the sampling rate and the maximum input signal frequency that the circuit can operate at. The S/H circuitry was tested at 2 GHz sampling rate (0.5 ns clock period) with a 1 GHz input sine wave signal. The output of the S/H can be seen in Figure 42. The output does not remain constant for the appropriate time during the clock cycle. The proper operation of the circuit should be obtained by readjusting the source voltage, Vs, and the high and low clock voltages. The adjustments were not made during this thesis due to time constraints.

5.2 Comparator Simulations.

The parameters that characterize comparator performance are sensitivity, sampling speed, rise and fall times, power consumption, logic swing, and source current value. The sensitivity of the comparator is defined as half of the maximum peak-to-peak voltage swing for proper comparator operation. The sensitivity of the fabricated transistors in [9] is 1 mV at 1 Gs/s and 200 mV at 10 Gs/s. All sensitivity measurements were taken with a sampling rate of 1 Gs/s. The maximum sampling rate (MSR) was found by running simulations starting at 1 GHz (1 ns clock period) and then running successive simulations at 2 GHz, 5 GHz, and 10 GHz. For all circuits, the rise (τ_r) and fall times (τ_f) were measured from the 10% and 90% marks of the output signal.

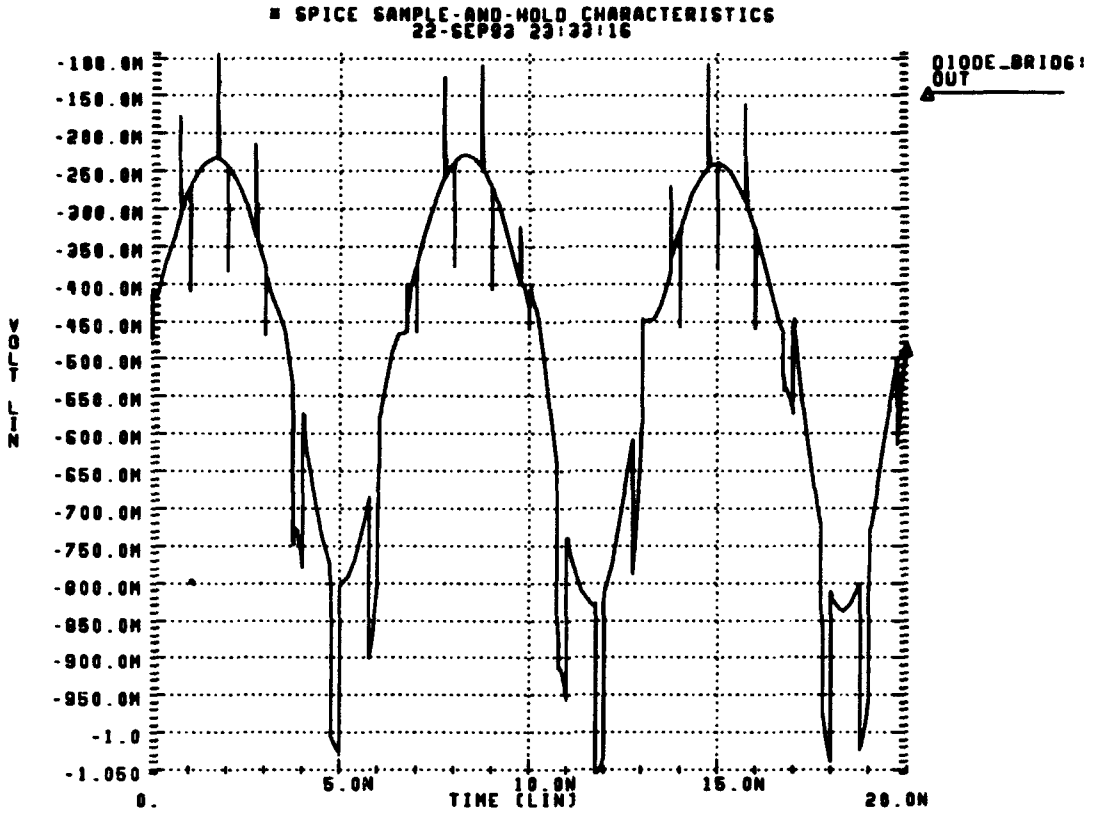


Figure 42. Simulations of S/H output with 1 GHz input and 2 Gs/s sampling frequency.

The simultated sensitivity, power dissipation, logic swing, current source, and delays for the comparator are shown in Table 5 for the three different HBT models . The maximum sampling rates were limited only by the sampling frequency and the associated rise and fall times of the clock signal. Therefore, the MSR was not included in Table 5. The simulations were performed using a 120 fF load with a fanout of two 3-input NOR gates, similar to the actual load of a comparator in a parallel ADC. The current source was implemented using an HBT driven by a voltage source. R_S was set to 100 Ω to conserve space. All comparator simulations used 50 ps rise and fall times for the clock signals. The output (OUTPUT) of the series-gated CML comparator using the Rockwell HBT SPICE parameters is shown in Figure 43. This follows the predicted output in the comparator operational diagram in Figure 26.

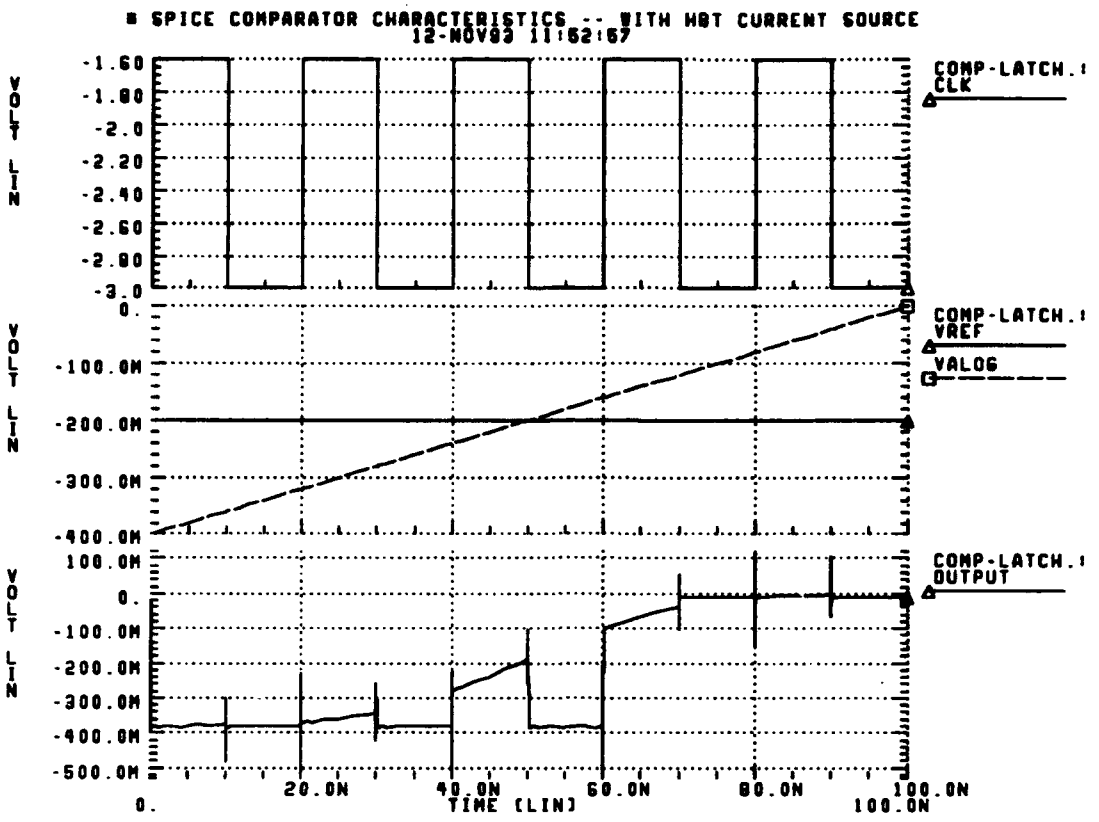


Figure 43. Operational diagram from HSPICE for series-gated CML comparator.

Table 5. Performance parameters for the MS series-gated comparator with fanout=2, 120 fF load, 50 ps rise and fall times for clock.

Comparator	Sensitivity (mV)	τ_r (ps)	τ_f (ps)	Power (mW)	Logic swing (mV)	I_S (mA)
Wang	2.2	321	275	9.0	362	1.0006
Fellows	2.3	230	196	9.0	358	1.0001
Rockwell mod6	1.2	238	204	9.0	377	1.0002

The master-slave (MS) configuration for the series-gated CML comparator created an output signal with more stability and less noise than the single series-gated comparator. The output (OUTPUT) of the MS configuration is shown in Figure 44. The output functioned as predicted in Figure 29.

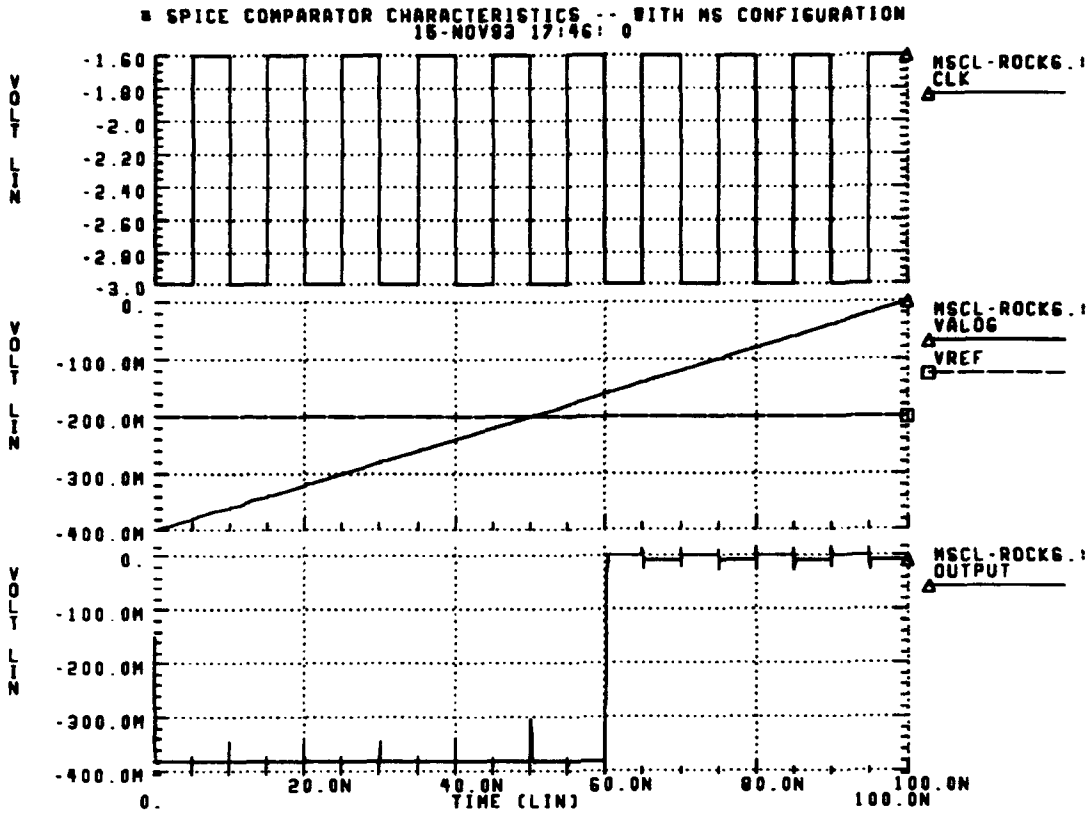


Figure 44. Operational diagram from HSPICE for MS series-gated CML comparator.

5.3 NOR/OR Gate Simulations

The 2-input NOR/OR gate performance parameters are the propagation delay, rise and fall times, and power dissipation of the circuit. The input signals were implemented with rise and fall times typical for a comparator with a fanout of three 3-input NOR gates, and a clock rise and fall times of 50 ps. The current source was set using R_S=100 Ω. There appeared to be a lot of noise at the output of the NOR/OR gates in the ADC simulations, so a voltage transfer characteristic (VTC) was produced to determine the noise margins of the circuit. Holding one input to -0.4 volts, the other input was raised from -0.4 volts to 0 volts until the output of the gate changed. The VTC curve for the 2-input NOR gate is shown in Figure 45.

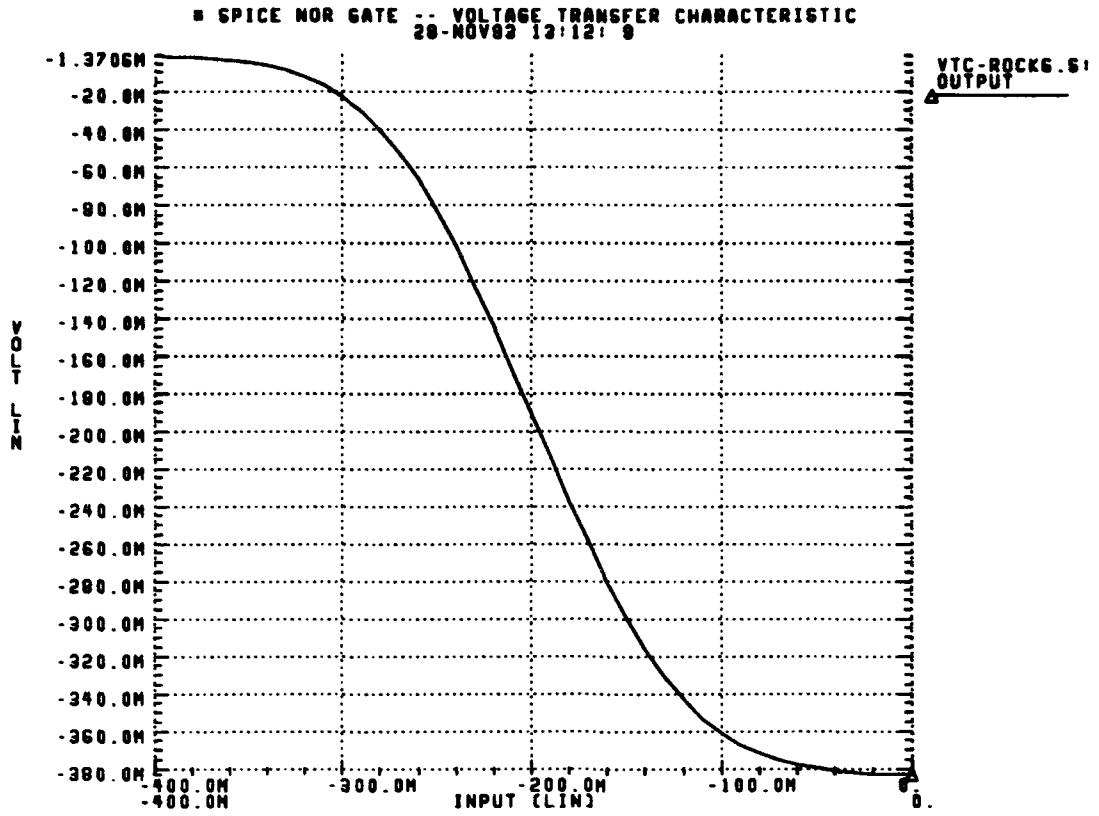


Figure 45. Voltage transfer characteristic for 2-input NOR/OR gate.

The VTC curve for the Fellows model yielded a low noise margin of 25 mV, due to the low current source with R_S=1 kΩ.. To increase the noise margin, the bias voltage, V_S, was increased to provide a larger current value through the circuit. Using Table 3, the bias voltage was increased to -1.95 V to achieve a 1 mA current at the emitter of the current source. However, the current at the collector was not checked to see if it was similar to the emitter current. The low noise margin was improved to 77 mV, while decreasing NM_H from 118 mV to 102 mV.

Table 6 shows the performance of the 2-input NOR gate without a load and an input signal with a 1 ps rise time. The rise and fall times for the clock circuitry was

obtained using this chart. It was assumed that any clock circuitry would be able to perform at the rate equivalent to the NOR gate.

Table 7 shows the performance of the 2-input NOR gate. The gate was simulated with a fanout of three 8-input OR gates, a 120 fF load, input signals with 180 ps rise times, and R_S set to 100 Ω. Simulations of the latched quantizers have shown that the actual propagation delays for the internal NOR gates range from approximately 30-70 ps.

Table 6. Performance parameters for 2-input CML NOR gate without load, R_S=1 kΩ.

NOR gate (2-input)	τ_D (ps)	τ_r (ps)	τ_f (ps)	Power (mW)	NM_H (mV)	NM_L (mV)
Wang	26	47	40	4.53	118	84
Fellows	13	22	23	3.76	118	29
Rockwell mod6	14	24	20	4.57	108	109

Table 7. Parameters for 2-input NOR with fanout=3, 120 fF load, 180 ps input rise time, and R_S=100 Ω.

NOR gate (2-input)	τ_D (ps)	τ_r (ps)	τ_f (ps)	Power (mW)	NM_H (mV)	NM_L (mV)
Wang	63	242	244	4.50	101	85
Fellows	51	233	235	4.50	100	80
Rockwell mod6	52	233	236	4.50	112	100

The propagation delay for the NOR gates was measured by taking the average of the rise and fall propagation delays. The results of the 3-input NOR gate with a fan-out of three 8-input NOR gates, R_S=100 Ω, 180 ps input rise times, and a 120 fF load is shown in Table 8 with the FET-FET technology researched by LaRue in 1990 [28]. The power-

delay product (PDP) shows that for the power expended driving the HBT NOR gate, the low delay achieves the same PDP.

Table 8. Performance results for the 3-input NOR gate with fanout=3, R_S=100 Ω, 120 fF load, and 180 ps input rise times.

NOR gate (3-input)	τ_D (ps)	τ_r (ps)	τ_f (ps)	Power (mW)	NM_H (mV)	NM_L (mV)	PDP (fJ)
LaRue [28]	300	-	-	0.8	-	-	240
Wang	85	312	274	4.50	100	85	382
Fellows	66	267	260	4.50	100	80	297
Rockwell mod6	64	263	253	4.50	110	100	288

5.4 8-input OR Gate Simulations

The 8-input OR gate has the similar performance parameters to the comparator. The sensitivity and current source were the same as the comparator, and are not shown in this section. The clock that was used to latch these circuits had a similar period and duty cycle as the primary clock for the comparators, but it was non-overlapping with the primary clock cycle. This was needed to allow the signal to propagate through to the encoding stage before the output was latched. Since the NOR gate delays were less than 70 ps, the signal should have enough time to propagate through with a sampling rate below 10 GHz (100 ps cycle). A operational diagram of the clock cycle is shown in Figure 46. The maximum sampling rate for the simulated latched OR gate was limited only by the clock rise and fall times. The performance parameters for the series-gated CML 8-input OR gate with R_S=1 kΩ, a 120 fF load, and 270 ps input rise times, which are similar to the rise and fall times of the 3-input NOR gate, are shown in Table 9.

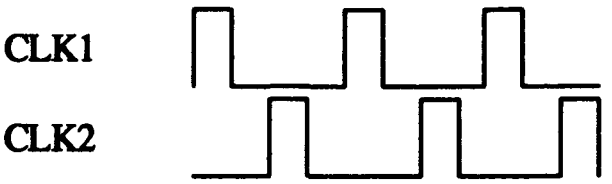


Figure 46. Timing diagram for CLK1 and CLK2.

Table 9. Performance parameters of 8-input CML OR gate with 120 fF load, R_S=1 kΩ, 50 ps rise and fall times for clock.

8-input OR gate	τ_r (ps)	τ_f (ps)	Logic swing (mV)	Power (mW)
Wang	411	412	364	9.06
Fellows	374	427	244	9.01
Rockwell mod6	376	408	383	9.12

As can be seen from Table 9, the Fellows model had a 244 mV logic swing, even with the -1.95 V bias voltage. Unfortunately, the increase in bias voltage did not solve the low logic swing at the output. The minimum output was dropping to -244 mV instead of the expected 350-400 mV drop exhibited by the other models. After checking the base current and collector current to the transistor that was being used as a current source, it was discovered that the input current at the collector was only 0.6 mA, where the output current at the emitter was 1 mA. Previously, the current had only been checked between the emitter and R_S, which provided a 1 mA reading. This can be explained by comparing the I-V characteristics for the Fellows model and the Rockwell model, which are located in Figures 14 and 15. The Rockwell model has an offset voltage of 80 mV, where as the Fellows model has a offset of almost 300 mV. This indicates that the Fellows model will require a larger voltage between the collector and emitter before it reaches the forward active region. After finding the simulation values of the voltage between the collector and

emitter, it was discovered that V_{CE} for the Rockwell models was 0.54 V, which is enough to put it in the forward active mode. The Fellows model had V_{CE}=0.40 V, which leaves it in the saturation region. This creates instability in the current source, since minor fluctuations in V_{CE} may bring about large changes in the collector current. Also, looking at the Gummel plots of Figure 16 and 17 offer another insight into the behavior of the Fellows model. If the emitter current of both the Fellows model and the Rockwell model were assumed to be equal at 1 mA, which means the voltage drop across R_S were the same, the voltage across the base and emitter, V_{BE}, would be the same for both devices, given that the bias voltages, V_S, were the same. Looking at the Gummel plots, it can be seen that for a given V_{BE}, both the collector current and the current gain (I_C/I_B) is going to be less for the Fellows model than for the Rockwell model. Because of this problem, R_S was changed to 100 so that a different voltage was present between the base and emitter, which had a direct impact on the output current. Also, lowering the resistance of R_S reduces the area that must be consumed by Nichrome resistors. Therefore, the 100 Ω resistance for R_S was chosen as a better configuration. The bias voltages that were optimized to produce 1 mA using R_S=100 Ω were listed with the bias voltages that produce 1 mA for R_S=1 kΩ in Table 3. The 8-input OR gate simulations using R_S=100 Ω is shown in Table 10.

5.5 Latched Quantizer Simulations

An ADC consists of a sample-and-hold, comparators, NOR gates, and a latched encoding stage. A quantizer is similar to the ADC, but does not contain output latches or a sample-and-hold. The performance parameters of the quantizer are the rise and fall times, as well as the maximum sampling rate and power dissipation. The voltages at the four latched outputs are shown in Figure 47. The reference voltages were divided into 16 equal parts, and the analog input was raised from -1.7 V to 0 V. The performance characteristics are shown in Table 11.

Table 10. Performance parameters of 8-input CML OR gate with 120 fF load, R_s=100 Ω, 50 ps rise and fall times for clock.

8-input OR gate	τ_r (ps)	τ_f (ps)	Logic swing (mV)	Power (mW)
Wang	411	412	364	9.06
Fellows	374	427	244	9.01
Rockwell mod6	376	408	383	9.12

5.6 Mixer Simulations

The output gain and the output frequency were the two main characteristics that were checked to determine proper operation of the four-quadrant double-balanced mixer. The output of the low-pass filter was initially measured for gain and frequency. A comparison between the output of the opamp and the output of the low-pass filter is shown in Figure 48. The graph shows that the signal stabilizes into a 1 GHz frequency as expected, and the amplitude is over 15 times that of the input signal (RF). Fourier analysis was performed during simulation to determine the harmonic distortion of the signal, and voltage measurement techniques were used to determine the gain, as well as S-parameter analysis. S-parameter simulations reveal that the gain, S_{21}, is approximately +5 dB through the Gilbert cell multiplier, before the signal is amplified by the opamp. This gain is similar to the +9 dB gain at the output of the filter, but is expected to be larger since it is before the filter. The discrepancy may be accounted for by the ideal opamp. Transmission of the signal may be impaired due to the unrealistic parameters of the opamp. When an ac analysis was performed on the network with the RF port as the input, and the output of the opamp as the output port, S_{21} was given as -200 dB, which indicates isolation. The distortion and gain of the signal at both the output of the opamp and filter are tabulated in Table 12.

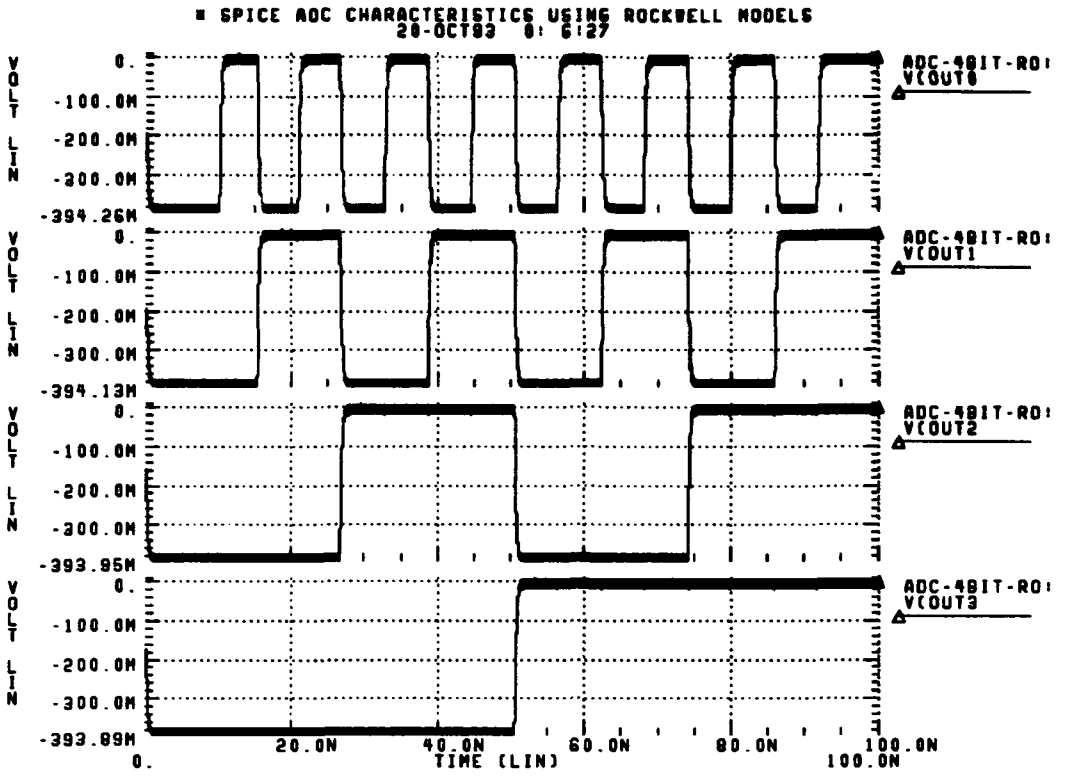


Figure 47. Output voltages for 4-bit quantizer using Rockwell HBT model.

Table 11. Performance parameters of latched quantizers.

Quantizer	τ_r (ps)	τ_f (ps)	MSR (GHz)	Power (mW)
Wang	500	455	-	250
Fellows	445	325	1	250
Rockwell mod6	440	320	1	250

Table 12. Performance parameters of mixer.

Configuration	Gain (dB)	Total Harmonic Distortion (%)
IF-out (before filter)	+26	16
OUTPUT (after filter)	+9	1

5.7 Extraction Results

The initial step of trying to extract the HBT from a Magic layout involved trying to implement a layer in the Magic technology file that was extracted as a transistor. The second step involved manipulating the layout information in the *.ext* files to output the collector, base, and emitter nodes for simulation. The last step involved attempting to extract parasitic and Nichrome resistances into a netlist file for simulation. The first two steps were successfully completed, but the third was not.

5.7.1 HBT Technology File. The HBT Magic technology file was changed so that it interpreted emitter layers as transistors in the Magic layout. The emitter is interpreted as a gate, the base as a source, and the collector layer is the substrate connection. This works well if the substrate does not have to be biased. If the transistor substrate needs to be biased, a different extraction statement in the extract section of the technology section will have to be implemented.

5.7.2 Code Adaptation. The *ext2spice* conversion program was modified to distinguish between HBTs and FETs in the Magic extraction file. The UNIX shell script *ext2hsp* will create an HSPICE netlist containing transistors and parasitic capacitances. This was accomplished by adding an conditional statement to the *fetVisit* subroutine.

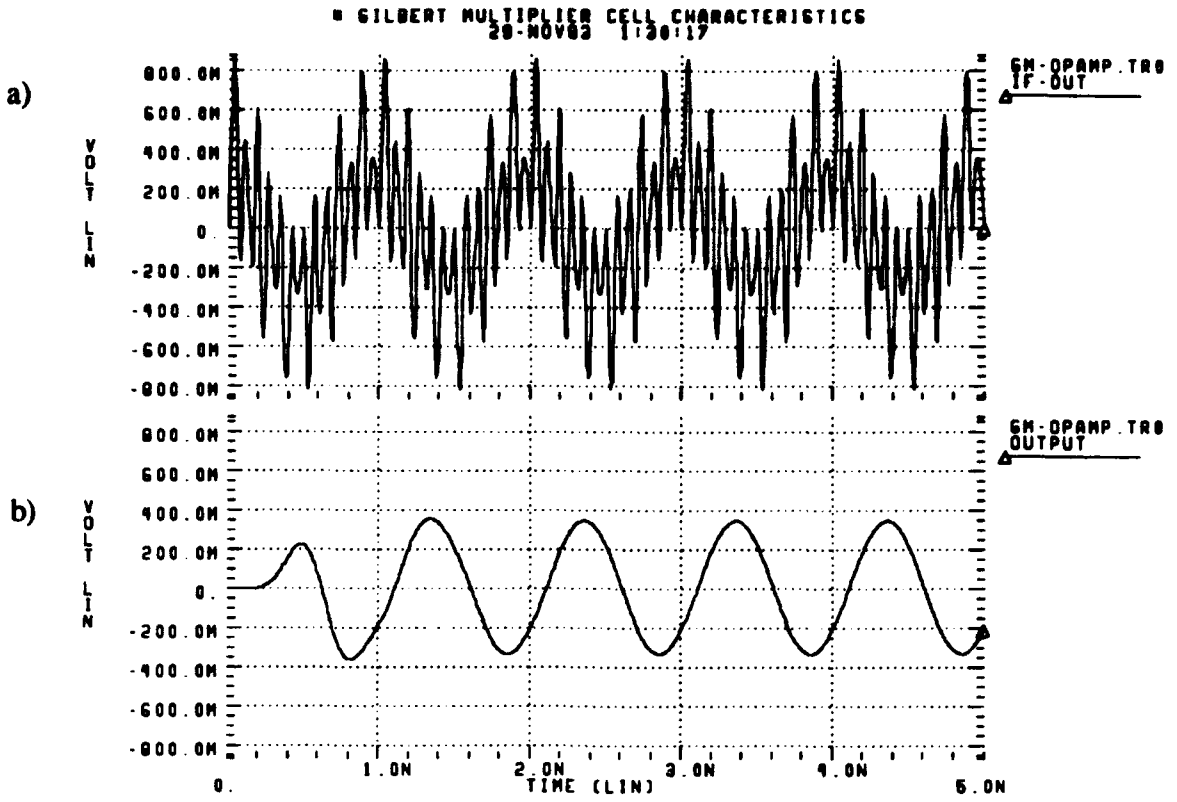


Figure 48. a) Output signal from opamp, b) output signal from low-pass filter.

5.7.3 Resistance Extraction. The resistance extraction failed due to Magic's inability to find the transistors during the *:extresis* command. This may be because the *ext2sim* program does not produce the correct information in the *.sim*, *.al* or *.nodes* files. The reasons for the failure is not certain at this time.

5.8 Summary

The results of the HSPICE simulations indicate that the ADC will operate at a sampling rate of 1 GHz, which is comparable to those listed in the literature review. The power dissipation is 250 mW, which is reasonable for CML configured systems. The propagation delays of the NOR/OR gate indicate potential for high-speed digital circuits

with values under 70 ps, since typical gates implemented in GaAs FET technology give delays three times as long.

The results of HSPICE simulation show that the mixer produces a 1 GHz signal from a 7 GHz radio frequency (RF) signal and a local oscillator (LO) with a 6 GHz frequency. The gain was found to be +9 dB at the output of the filter with less than 1 percent harmonic distortion.

VI. Conclusions

6.1 Summary

The objective of this thesis was to design and simulate the components of small-scale integrated circuits implemented using HBT technology. The circuits that were designed and simulated are the components of a 4-bit parallel analog-to-digital converter (ADC) and a four-quadrant analog mixer/multiplier. The development of the ADC investigated the dc performance of the HBT transistor for both analog and digital applications. The development of the mixer investigated the high-frequency response of the HBT.

The 4-bit parallel ADC operated at a clock rate of over 1 GHz when implemented using the adapted Rockwell and Fellows HBT models. The digital NOR gates of the ADC show a propagation delay of less than 70 ps with a 120 pF capacitive load, no fanout, and inputs with rise and fall times equivalent to comparator output delays. This is accomplished with noise margins of at least 80 mV. The series-gated current-mode logic (CML) configuration shows promise for implementing latched components. CML had the versatility to implement both the comparator and the 8-input OR gate. The simulated maximum sampling rate of the comparator and 8-input OR gate was only limited by the rise and fall times of the clock signal. The CML components were designed with a 1 mA current source and used 400 Ω load resistors to create a 400 mV logic swing. The 1 mA current source and the 4.5 V power-to-ground voltage difference led to 4.5 mW power dissipation rate per component and a 252 mW dissipation for the active components of the 4-bit quantizer.

The four-quadrant double-balanced mixer based on the Gilbert cell multiplier with a operational amplifier output produced a 1 GHz output signal with 16 percent harmonic distortion and +26 dB gain. These parameters were obtained using a 7 GHz radio frequency (RF) signal and a 6 GHz local oscillator (LO). When a low-pass passive 1 dB

Chebyshev filter was connected to the intermediate frequency (IF) output, the RF signal, which was the dominant distortion frequency, was filtered out. This provided an IF signal with a +9 dB gain and harmonic distortion of less than 1 percent.

The Magic technology file was altered so that it could extract HBTs. The conversion program *ext2spice* was changed so that it can distinguish between FETs and HBTs and output the collector, base, and emitter nodes in the BJT format for HSPICE. This allows HBTs and associated capacitances to be extracted into a HSPICE netlist. An attempt was made to adapt the conversion program *ext2sim* so that resistors could be extracted. However, the Magic resistance extractor failed to recognize the HBT layout configuration.

6.2 Recommendations

This section details some of the directions that the research should take in the future. Direction is provided in the areas of ADC configuration, digital components, high-frequency integrated circuits, extraction techniques, and circuit layout.

1) *Implement an operational amplifier using HBT technology.* The design of the mixer depends on the ideal performance of the opamp. While ideal simulations may produce optimistic results, simulations reveal that the design appears correct and can be altered for non-ideal performance. The opamp used in the simulations used a gain of 5, with a feedback resistor of 4 kΩ. The 4 kΩ resistor and 1 kΩ resistors will occupy a large amount of area in the circuit if NiCr resistors are used. If the epilayer or WSiN resistors are used, the potential for greater variance from the standard resistivities is introduced. This means that some compromises have to be made in the implementation of the opamp.

2) *Fabricate and test the 4-bit parallel ADC and the mixer.* This thesis effort was intended to prepare circuits for fabrication. A follow-on thesis would obtain an extracted

netlist for the Magic layouts for the ADC from Rockwell and then perform a layout versus schematic check prior to fabrication to ensure proper operation of the circuit. If the chips were fabricated, a full range of tests would be executed such as delay measurements, gain measurements, and Nyquist tests. Nary has offered the use of the testing equipment at Rockwell for testing HBT implemented circuits for future theses. The mixer could be fabricated at Wright Laboratory using their HBT, which is suited for microwave applications.

3) *Modify the resistance extraction code.* There are other ways to modify the resistance extraction code that have not been examined. The internal Magic code uses a subroutine *killnode* that splits a large lumped resistance into two nodes separated by a resistor. If this subroutine can be implemented in the *ext2spice* program, the need for using the Magic resistance extractor could be eliminated from the loop. This can be done since the lumped resistance value for each node is listed in the *.ext* files. This would not affect the FET extraction, since resistances for the CMOS technology file could also be extracted using this method. Also, the configuration of the HBT in the HBT technology file may be causing the recognition problems. In that case, the configuration of the HBT can be altered to look more like a FET so that the resistance extractor will recognize it using the *:extresist* command.

4) *Add on-chip clock circuitry.* Some research has already integrated on-chip clocks into components. This could reduce clock skew problems that occur due to long interconnect lines from importing the clock signals from off chip. Also, since the circuits require high sampling rates, the clock needs to be implemented in the same technology to provide the 50 ps rise and fall times on the clock pulse. The sample-and-hold component needs to be added for higher frequency inputs. The bias voltages, V_S, and clock voltages, CLK and

CLK_BAR, may need to be buffered using emitter followers to increase the current drive to the gates.

5) *Investigate the minimization of logic swings for reduced power consumption.* The output logic swing, 400 mV, that was used in this thesis effort is larger than current logic swings in use at Rockwell. The logic swing can be affected by lowering the resistive load, R_L, by reducing the current source, or by reducing the power-to-ground voltage difference. However, since the noise margins are sensitive to any reductions in the current, the margins must be watched closely. The large amount of noise in the circuit simulations may make logic swing reduction difficult.

6) *Redesign the Wright Laboratory Magic layout using less conservative design rules.* The design rules for the Wright Laboratory HBT process were conservative due to the goals driving their research. Their emphasis was placed on device research with a focus on analog, high-frequency microwave applications. Due to this emphasis, the design rules took into consideration the mutual inductance and capacitances that interconnections exhibit. For this reason, the metal line-to-line spacing was a conservative 10 μm, even between different types of metal. This caused the area of the ADC layout to expand considerably, and the affect can be seen by the dimensions of the final layout- 4819 μm by 6685 μm. Typical metal-to-metal spacing rules used in the SCMOS technology file exhibit the 3 to 4 μm spacing between similar metals and allow unrestricted overlapping of different metal layers with minimal impact on the performance of the circuit. The performance of digital SSI circuits are not effected by mutual or self inductance at low operational frequencies. However, mutual induction and internodal capacitance could become a bigger concern as the sampling frequencies increase in HBT circuits The area of the layout could possibly be reduced by half if less conservative design rules were placed in the design rule checker portion of the Wright Laboratory technology file. The

technology file used to implement the Wright Laboratory design rules is referenced in Appendix C.

7) *Get involved with other research projects.* The RISC processor being developed by McDonald using HBT technology [29], involves many digital components that could be designed at AFIT. The series-gated CML configuration should give a variety of logic functions that could be developed. Also, Wright Laboratory may be interested in developing devices more suitable for microwave applications, such as the mixer. Oscillators and high-power amplifiers might be another option that would interest Wright Laboratory. The digital radio frequency memory (DRFM) component used for electronic warfare (EW) purposes, uses a mixer and ADC as components for its implementation. This may mean that HBTs can play a role in this program, even if all the components of the DRFM cannot be produced using HBT technology. The fact that gallium arsenide is used as the semi-insulating substrate instead of a semiconducting substrate, such as silicon, may provide convenient integration of different devices such as HEMTs or GaAs FETs with HBTs in the future. Wright Laboratory is currently working on projects that will integrate HBTs with HEMTs on GaAs wafers. This process may not be available in the near future, however. Table 11 in Appendix F lists contacts who may be of assistance.

6.3 Conclusions

The three objectives of the thesis were all met to some degree. The HBT implemented 4-bit parallel ADC was simulated at high sampling rates, and can operate with high-frequency inputs using an sample-and-hold. The mixer was simulated using a Gilbert cell multiplier with a operational amplifier as an output stage, and a low-pass filter. The mixer has the ability to accept a high-frequency input and produce a intermediate frequency signal with little distortion. The extraction code can extract vertical HBTs and the parasitic capacitances associated with interconnects. The capabilities of the extraction

techniques and the development of the designed circuits indicate that HBT technology can be used to implement high-speed digital and analog integrated circuits.

Appendix A - ADC HSPICE Netlists

Appendix A contains the names of the HSPICE netlists for the ADC in Table 13, which are used for simulation which test the circuit configuration, and also contains the names of the subcircuits used in top-level simulations. The simulation files used to test individual components are found in subdirectories under the main project directory **~hbt/hspice** and the subcircuits are found in **~hbt/hspice/adc**. Table 14 contains the names of the top-level netlists for simulation.

Table 13. HSPICE filenames and location.

Component	Sub-directory	HSPICE sim.	HSPICE subcircuit
Sample-and-hold	samp_hold	S_H.sp	S_H.sub
diode bridge	samp_hold	diode_bridge.sp	diode_bridge.sub
output buffer	samp_hold	out_buf.sp	out_buf.sub
differential pair	comparator	diffpair.sp	None
comparator	comparator	comp-latch.sp	comp-latch.sub
2-input NOR gate	nor	nor2-ss.sp	nor2-ss.sub
3-input NOR gate	nor	nor3-ss.sp	nor3-ss.sub
8-input OR gate	or8	or8-enc.sp	or8-enc.sub
MS comparator	comp-latch	mscl.sp	mscl.sub
MS 8-input OR gt.	or8	msor8.sp	msor8.sub

Table 14. Top-level ADC HSPICE simulation files.

HSPICE HBT model	Sub-directory	HSPICE filename
Rockwell mod6	adc/rock	adc_4bit_ROCK6.sp
Fellows	jfell	adc_4bit_jfell.sp
Wang	kcw	adc_4bit_kcw.sp

The files that were used to verify transistor performance are found in **~hbt/hspice/iv-plots** and are listed in Table 15.

Table 15. Files to verify HBT performance.

Plot	Sub-directory	HSPICE sim.
I-V curves	iv-plots	kcw_iv.sp rock_iv.sp fell_iv.sp
Gummel plots	iv-plots	kcw_gum.sp rock_iv.sp fell_iv.sp

Appendix B - Mixer HSPICE Netlists

Appendix B contains the HSPICE netlists for the four-quadrant double balanced mixer. The files that are included are, in order:

1) Gilbert cell multiplier

2) Inverse hyperbolic tangent function

3) Passive low-pass 1-dB Chebyshev filter

1) Gilbert cell multiplier

```
* GILBERT Multiplier Cell Characteristics
* Author:  Scott F. Jokerst
* Date: 23 Jul 93
* Filename:  gm-opamp.sp
* This file includes a inverse-hyperbolic tangent function
* as an input stage to the RF input to increase
* the amplitude variation of the input voltages
* Technology:  Heterojunction Bipolar Transistor
* Description:  This file provides data for microwave
applications
* such as an analog multiplier/mixer implemented with a
* GILBERT multiplier cell using HBT models.
*-------------------------------------------------------
-------

*-----------------------------------------------
* Voltage Source   (+) node    (-) node    Value
*-----------------------------------------------

     VLO        LO1-in          0       AC sin (0 0.316 6GHz
0 0 0)
     VRF     RF1-in  0       AC sin (0 0.02 7GHz 0 0 0)
     Vin1    Vcc          0       10
     Vin2    Vee          0       -10

     Vcheck       IF-out  opout


** include inverse hyperbolic tangent function as input to
compensate for
** hyperbolic tagent function present at higher input
amplitudes.
** This will give the voltage amplitudes more freedom.
```

```
XRFin     RF1-in GND outplus outmin GND Vee inv-tanh

*-----------------------------------------------
* HBT      Coll    Base   Emitter        model
*-----------------------------------------------
Q11       GND  GND  q9c       T3u1d1f
Q12  GND  GND  q10c      T3u1d1f

Q9   q9c  LO1-in    q9e       T3u1d1f
Q10  q10c GND  q10e      T3u1d1f

R12  q9e  q13c 50
R13  q10e q13c 50

**********inv-hyp tang current source**************
Iinvt     q13c  Vee 2mA

*-----------------------------------------------
* Circuit Elements  (+) node    (-) node    Value
*-----------------------------------------------
     R2   Vcc    out1        400
     R1   Vcc    out1_bar    400

*-----------------------------------------------
* BJT   Collector     Base     Emitter    model
*-----------------------------------------------
  Q1        out1_bar q9c   q5c      T3u1d1f
  Q2        out1          q10c  q5c      T3u1d1f
  Q3        out1_bar q10c       q6c      T3u1d1f
  Q4          out1        q9c      q6c     T3u1d1f
  Q5    q5c          outplus  q5e      T3u1d1f
  Q6        q6c       outmin     q6e      T3u1d1f

** Add two resistors to the RF emitter resistors for
flexibility

     R10  q5e    upper        50
     R11  q6e    upper        50

**********Gilbert cell current source**************
Igils     upper     Vee  4mA

************opamp***************
R15  out1_bar out2_bar 1k
R16  out1  out2       1k
R17  out2_bar  GND     4k
Rfeedb  out2   IF-out      4k

Eopamp IF-out GND out2 out2_bar  MAX=+10 MIN=-10  5

* include low-pass filter to filter out RF and LO input
frequencies

x1 opout GND output      lpv8-filter
```

```
.include 'lpv8-filter.sub'
.include 'inv-tanh.sub'

.option brief post

.trans 1ns 5ns
.FOUR 1GHz V(out1)

.measure tran p2pIFout pp V(out1) from=2.45ns to=3.2ns
.measure tran p2pRFin  pp V(RF1-in) from=1.8ns to=1.95ns

.measure tran gain0 PARAM='20*log(p2pIFout/p2pRFin)'

.measure tran ip2p pp i(Vcheck) from=0.8ns to=1.8ns


**************measure S parameters- S21 is the output
gain*************

.ac DEC 10 10MEG 10GHz
.NET V(out1)  VRF  ROUT=50  RIN=50
.print AC S11(db) S12(db) S21(db) ZOUT Z11(M)

* Data to be collected:
*--------------------------------
*      Vce        Ib        Ic
*--------------------------------
*.print tran i(Vcheck1)

.prot

.model T3u1d1f  npn
  + BF   =    6.2943e+08   BR   =    0.1512       NF   =
1.1121
  + NR   =    1.00000      NE   =    1.8414       NC   =
1.4832
  + RB   =    43.2846      RE   =    33.6707      RC   =
55.00
  + IS   =    2.2354e-26   ISE  =    6.2691e-19   ISC  =
1e-17
  + CJE  =    9.8515e-15   MJE  =    .50          VJE  =
1.7018
  + CJC  =    1.119e-14    MJC  =    .50          VJC  =
1.3691
  + TF   =    9.5681e-13   TR   =    5.287e-10    XCJC =
0.2053
  + IKF  =    1.9e-03
.end
```

2) Inverse-hyperbolic tangent function

```
.protect
* INVERSE HYPERBOLIC TANGENT COMPONENT
* This input to LO-in will increase amplitude range of
inputs
* Author:  Scott F. Jokerst
* Date: 23 Jul 93
* Filename:  inv-tanh.sub
* Corrsponding VHDL File:  none
* Technology:  Heterojunction Bipolar Transistor
* Description:  This file provides a subcircuit for a
microwave applications
* circuits
*-------------------------------------------------------------
-------

.subckt inv-tanh inplus  inminus outplus outmin GND Vee

*-----------------------------------------------
* Circuit Elements  (+) node    (-) node    Value
*-----------------------------------------------
Q11       GND  GND  outplus        T3u1d1f
Q12  GND  GND  outmin          T3u1d1f

Q9   outplus   inplus    q9e       T3u1d1f
Q10  outmin    inminus   q10e      T3u1d1f

R1   q9e  q13c 50
R2   q10e q13c 50

I1   q13c Vee  4mA

.ends
.unprotect
```

3) Passive low-pass 1-dB Chebyshev filter

```
.protect
* LOWPASS FILTER Characteristics
* LOWPASS 8-pole 1-dB ripple Chebyshev FILTER for voltage
driven outputs
* Author:  Scott F. Jokerst
* Date: 23 Jul 93
* Filename:  lpv8-filter.sub
* Corrsponding VHDL File:  none
* Technology:  Heterojunction Bipolar Transistor
* Description:  This file provides a subcircuit for a
microwave applications
* circuit such as an analog multiplier/mixer implemented
with a
* GILBERT multiplier cell using HBT models.
*-------------------------------------------------------------
-------

.subckt lpv8-filter input GND output

*-----------------------------------------------
* Circuit Elements  (+) node    (-) node    Value
*-----------------------------------------------
R1 output GND  1.0
C1 output GND       57pF
L2 1 output    78.46pH
C3 1 GND       109pF
L4 2 1         90pH
C5 2 GND  114pF
L6 3 2         90.5pH
C7 3 GND  111.3pF
L8 input 3     72.8pH
.ends
.unprotect
```

Appendix C - Magic Cells

Appendix C contains the names of the Magic layout files in Table 16 which show the circuit configuration. These files are found in **~hbt/magic/wlmag** for the Wright Laboratory layouts and in **~hbt/magic/wlrock** for the Rockwell implementation.

Table 16. Magic implementation of components.

Component	Magic cell (wlhbt)	Magic cell (hbt)
Sample-and-hold	None	S_H.mag
HBT	dum1.mag	dum1.mag
differential pair	diffpair.mag	diffpair.mag
comparator	comp-latch.mag	comp-latch.mag
2-input NOR gate	nor2-ss.mag	nor2-ss.mag
3-input NOR gate	nor3-ss.mag	nor3-ss.mag
8-input OR gate	or8-ss.mag	or8-ss.mag
MS comparator	mscl.mag	mscl.mag
MS 8-input OR gt.	msor8.mag	msor8.mag
4-bit ADC w/overfl.	adc_4bit.mag	adc_4bit.mag

Appendix D - Magic Technology Files

Appendix D contains the reference to the Magic technology files that were used to produce the Wright Laboratory and Rockwell mask layouts. These technology files can be found in **~cad/magicv6/lib/magic/sys** and are listed in Table 17.

Table 17. Magic technology files and filenames.

Technology	Technology filename
Rockwell HBT	hbt.tech26
Wright Laboratory HBT	wlhbt.tech26

The technology files that are listed are, in order:

1) Rockwell HBT technology file

2) Wright Laboratory technology file

1) Rockwell HBT technology file

```
# 1 "hbt.tech"
```

```
#1 "hbt.tech"

tech
     hbt
end

planes
     active
     metal1
     metal2
     metal3
end

types
```

```
        active          active_area,act
     active          dum

/* I added a collector, base, and emitter layer.
     The collector is place on a different plane than the
emitter and
     base, because we will use it as the substrate
connection.
   Most of these additions can be found in the new
scmos.tech26 */


        metal1       collector,coll,col,co,cl
        active       emitter,emit,em
        active       pbase,pb

/* These are the contacts for the emitter,base and
collector*/

        metal1       collectorcontact,colcontact,colc,coc,clc
        active       emittercontact,emitcontact,emc
        active       pbasecontact,pbcontact,pbc

     metal1          metal_1,m1
     metal2          metal_2,m2
     metal3          metal_3,m3

     metal1          res,lres
        metal1           wsin,hres
     metal1          rcon
        metal1           wscon
     metal1          cap
     metal1          m1dum
     metal1          nogo
        metal2             via1,v1
        metal3             via2,v2
        metal3             pad
end

styles
     styletype mos

     active_area    2

     res       1

     wsin      3
     wsin      14

     rcon      1
     rcon      20
```

```
rcon        36

wscon               3
wscon               14
wscon               20
wscon               33

metal_1             20

nogo        2
nogo        12

m1dum               2
m1dum               20
m1dum               33

metal_2             21

metal_3             5

via1        20
via1        21
via1        32

via2        5
via2        21
via2        32

cap         1
cap         20
cap         21
cap         30

pad         5
pad         21
pad         32
pad         33

error_s             42
error_p             42
error_ps    42

/* These are the styles for the new layers*/

    pbase           15
    pbc             15
    pbc             20
    pbc             32
    emit            16
    emc             16
    emc             20
    emc             32
    col             3
    clc             3
```

```
    clc          20
    clc          32

end

contact
     m1dum      dum  m1
     via1 m1    m2
        via2    m2   m3

/* Create contacts for the emitter and base*/

     emc          emit    metal_1
     pbc          pbase   metal_1

end

compose

     paint      res  m1   rcon
     paint      m1   res  rcon
     paint      rcon res  rcon
     paint      rcon m1   rcon

     paint      wsin m1   wscon
     paint      m1   wsin wscon
     paint      wscon     wsin wscon
     paint      wscon     m1   wscon

     paint      pad  m3   pad
     paint      pad  m2   pad

     paint      cap  m2   cap
     paint      cap  m1   cap

     erase      rcon m1   res
     erase      rcon res  m1

     erase      wscon     m1   wsin
     erase      wscon     wsin m1

     erase      pad  m2   pad
     erase      pad  m3   pad

/* Compose the collector base and emitter contacts*/

    paint       clc     col     clc
    paint       emc     emit    emc
    paint       emc     pbase   emc

end

connect
```

```
/* I added the collector contact (clc) to the metal_1
connect line*/
     rcon       metal_1
     metal_1          via1,pad,res,wsin,cap,m1dum,clc
     metal_2          via1,via2,pad
     metal_3          via2,pad
     via1       via2
/* I added the collector base and emitter contacts */
    pbase                pbc
    collector            clc
    emitter              emc

end

cifoutput
     style           lambda
     scalefactor     50


        layer DIW pad
          shrink 700
          calma 6 1

     layer RES res,rcon,lres
          calma 8 1

     layer 1LM pad
          shrink 500
          or cap,m1,via1,rcon,wscon,m1dum
          calma 9 1

     layer VIN pad
          shrink 850
          or via1
          shrink 50
          calma 10 1

     layer 2LM cap
          grow 300
          or pad
          shrink 250
          or m2,via1,via2
          calma 11 1

     layer SCR pad
          shrink 1050
          calma 12 1

     layer VI2 pad
          shrink 500
          or via2
          shrink 150
          calma 13 1
```

```
      layer 3LM m3,via2,pad
           calma 14 1

      layer VIP pad
           shrink 750
           or via1
           shrink    50
           or cap
           calma 16 1

      layer WSIN wsin,wscon,hres
           calma 18 1

      layer FNE pad
           shrink 1250
           calma 22 1

      layer ACT active
           calma 30 1

end

cifinput
end

mzrouter
end

drc
end

extract
/* This section is completely new*/
style lambda=0.5

    lambda      100


    step        100


    resist     res                    50000
    resist      dum,act                      25300
    resist      metal_1                            50
    resist      metal_2                            20


    areacap     metal_1                        24
    areacap     metal_2                              19

    overlap     metal_2  metal_1                      45

/* The next statement has three main points
     1. The emitter-base junction indicates a transistor
```

```
     2. The model "qnpn" can be changed to "hbt" for
simulation
     3. The extractor looks at the collector as a substrate
connection
*/
    fet emit,emc/act pbase,pbc/act   1  nhbt  Error!  coll 0
0

end

wiring
   contact  via1   6  m1  0  m2  0
   contact  via2  14  m2  0  m3  0
end

router
end

plowing
end

plot
     style     versatec

        act,nogo \
            0000 4242 6666 0000 \
            0000 2424 6666 0000 \
            0000 4242 6666 0000 \
            0000 2424 6666 0000


        res,rcon \
                07c0 0f80 1f00 3e00 \
                7c00 f800 f001 e003 \
                c007 800f 001f 003e \
                00c7 00f8 01f0 03e0

        wsin,wscon \
            1f00 0f80 07c0 03e0 \
            01f0 00f8 007c 003e \
            001f 800f c007 e003 \
            f001 f800 7c00 3e00

        cap \
                8080 0000 0000 0000 \
                0808 0000 0000 0000 \
                8080 0000 0000 0000 \
                0808 0000 0000 0000

        rcon \
            c3c3 c3c3 0000 0000 \
            0000 0000 c3c3 c3c3 \
            c3c3 c3c3 0000 0000 \
            0000 0000 c3c3 c3c3
```

```
        wscon \
            c3c3 c3c3 0000 0000 \
            0000 0000 c3c3 c3c3 \
            c3c3 c3c3 0000 0000 \
            0000 0000 c3c3 c3c3

        m1,m1dum,via1/metal1,rcon/metal1,wscon/metal1,pad \
            8080 0000 0000 0000 \
            0808 0000 0000 0000 \
            8080 0000 0000 0000 \
            0808 0000 0000 0000

        pad \
            0000 0000 1c1c 3e3e \
            3636 3e3e 1c1c 0000 \
            0000 0000 1c1c 3e3e \
            3636 3e3e 1c1c 0000

        m2,via2,pad \
            0000 1111 0000 0000 \
            0000 1111 0000 0000 \
            0000 1111 0000 0000 \
            0000 1111 0000 0000

        m3,pad \
            2020 2020 2020 2020 \
            2020 2020 2020 2020 \
            0000 0000 0000 0000 \
            0000 0000 0000 0000

        via1,via2,rcon,wscon,v1,v2    X

/* The collector base and emitter layers are given formats
here*/

    col,clc \
            0808 1414 2222 4141 \
            8080 4040 2020 1010 \
            0808 1414 2222 4141 \
            8080 4040 2020 1010

    clc/metal1,emc/metal1,pbc/metal1\
            8080 0000 0000 0000 \
            0808 0000 0000 0000 \
            8080 0000 0000 0000 \
            0808 0000 0000 0000

        clc,emc,pbc  X

    style gremlin
         active          2
         lres       9
         m3         19
```

```
            cap         22
            via1        24
            via2        15
            metal_1             30
            metal_2             31
end
```

2) Wright Laboratory technology file

The technology file for the Wright Laboratory layout is the same as the Rockwell layout except for the design rule section, which is presented below.

```
drc

         spacing act act 20 touching_ok \
        "1.1:  Transistors must be at least 20 microns apart
(% lambda)"

        width res 15 \
        "8.1 and 8.2:  EPI must be at least 15 microns wide
(% lambda)"

        spacing res res 20 touching_ok \
        "8.3:  Minimum EPI-to-EPI spacing is 20 microns (%
lambda)"

        spacing m1 m1 10 touching_ok \
        "8.3:  Minimum m1-m1 spacing is 10 microns (%
lambda)"

        spacing m1 act 10 touching_ok \
        "8.3:  Minimum m1-act spacing is 10 microns (%
lambda)"

        spacing m2 m2 10 touching_ok \
        "8.3:  Minimum m2-m2 spacing is 10 microns (%
lambda)"

        width   rcon  6 \
        "8.5:  Resistor contact must be at least 6 by 15
microns (% lambda)"

        edge res ohmic 1 ohmic,con1 0 1 \
        "8.6: Ohmic layer overlap of active resistor must be
1 micron (% lambda)"

        edge con1 m1 2 m1 0 2 \
        "8.6: M1 overlap of resistor contact must be 3
microns (% lambda)"

        spacing rcon,res act 20 touching_illegal \
        "8.8: EPI to active spacing must be at least 20
microns (% lambda)"

        width  via1 6 \
        "10.1: Via 1 must be at least 6 by 6 microns (% by %
lambda)"
```

```
        width cap 5 \
        "11.1: Polyimide via must be at least 5 by 5 microns
(% by % lambda)"

        spacing m2,v1,v2 m2,v1,v2 10 touching_ok \
        "12.2: M2 minimum spacing is 10 microns (% lambda)"


        width v1 6 \
        "13.1:  Minimum via dimension is 6 microns (%%%
lambda)"


        spacing v1 v1 10 touching_ok \
        "13.2: Minimum via spacing is 10 microns (%%%
lambda)"

end
```

Appendix E - fetVisit Subroutine

Appendix E contains the subroutine in ext2spice that was alted to extract HBTs for high-speed performance.

fetVisit:

```
fetVisit(fet, hierName, trans, l, w)
    Fet *fet;           /* Fet being output */
    HierName *hierName; /* Hierarchical path down to this
fet */
    Transform *trans;   /* Coordinate transform for output
*/
    int l, w;
{
    FetTerm *gate, *source, *drain;
    int gNode, sNode, dNode, subsNode;
    int scale;
    Rect r;

    /* If no terminals, can't do much of anything */
    if (fet->fet_nterm < 2)
        return 0;

    /* If only two terminals, connect the source to the
drain */
    gate = &fet->fet_terms[0];
    source = drain = &fet->fet_terms[1];
    if (fet->fet_nterm >= 3)
        drain = &fet->fet_terms[2];

    /*
     * Find the node numbers for the four fet terminals.
     * If any of the nodes have a lumped resistance greater
     * than the threshold, output a resistor between the fet
     * terminal and the node whose value is half of the
lumped
     * resistor.
     */
    dNode = esFetHier(hierName, drain->fterm_node),
    gNode = esFetHier(hierName, gate->fterm_node),
    sNode = esFetHier(hierName, source->fterm_node),
    subsNode = esFetHier(hierName, fet->fet_subsnode);

    /*
     * If fet is an HBT, then print the BJT format for
HSPICE
     */
```

```
    if (!strcmp(EFFetTypes[fet->fet_type], "nhbt"))
       {
       (void) fprintf(esSpiceF, "Q%d %d %d %d %s\n",
                esFetNum++, subsNode, sNode, gNode,
                EFFetTypes[fet->fet_type]);
       return 0;
       }

    /*
     * If fet is an FET, then print the FET format for
HSPICE
     */

    (void) fprintf(esSpiceF, "M%d %d %d %d %d %s",
                esFetNum++, dNode, gNode, sNode, subsNode,
                EFFetTypes[fet->fet_type]);

    /*
     * Scale L and W appropriately by the same amount as
distance
     * values in the transform.  The transform will have a
scale
     * different from 1 only in the case when the scale
factors of
     * some of the .ext files differed, making it necessary
to scale
     * all dimensions explicitly instead of having a single
scale
     * factor at the beginning of the .sim file.
     *
     * Multiply by overall scalefactor to get centimicrons.
     */
    GeoTransRect(trans, &fet->fet_rect, &r);
    scale = GeoScale(trans) * EFScale;
    l *= scale;
    w *= scale;
    (void) fprintf(esSpiceF, " L=%.1fU W=%.1fU\n",
                ((double) l) / 100.0, ((double) w) / 100.0);

    return 0;
}
```

Appendix F - Contacts

Appendix F contains information in Table 18 about contacts who have offered assistance throughout the research effort.

Table 18. Contacts for modeling and fabrication assistance.

Name, Organization	Phone	E-mail	Assitance
Bayraktaroglu, Burhan-WL	(513)255-1733	--	HBT geometries
Lemnios, Zachery-ARPA	(703)696-2278	--	MTC fabrication
Mehalic, Mark-AFIT	(513)255-5276	mmehalic@eris.afit.af.mil	Thesis advisor
Mehrotra, Depak-MTC	(805)375-1237	--	MTC fabrication
Nary, Kevin-Rockwell SC	(805)373-4643	krn@risc.rockwell.com	Magic tech file, SC fabrication
Via, David-WL	(513)255-8629	dvia@elmo.el.wpafb.mil	WL mask layout
Wang, K. C.-Rockwell SC	(805)373-4143	kcw@risc.rockwell.com	HBT proj. chair.

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A 4-bit parallel analog-to-digital converter (ADC) and a four-quadrant double-balanced mixer were designed and simulated using heterojunction bipolar transistor (HBT) technology to test the dc and high-frequency characteristics of HBTs. HSPICE simulations of small-scale components and the large-scale ADC operated within expected ranges. The ADC implemented with the Rockwell HBT model operated at a sampling rate of over 1 GHz, and the Fellows model also operated at a 1 GHz sampling rate. The mixer produced an intermediate frequency (IF) signal using radio frequency (RF) and local oscillator (LO) inputs. The circuit produced a +9 dB power gain with less than one percent harmonic distortion and shows potential for microwave applications.

In order to facilitate the fabrication of HBT circuits, a Magic technology file was developed to lay out HBTs and extract the transistors for the purpose of doing a layout versus schematic check. The extraction software was altered to recognize HBTs in the extracted file. The program ext2spice successfully identified HBTs and converted the transistors, as well as parasitic capacitances, into an HSPICE netlist. Since load resistors determine the output logic swing in current-mode logic, an attempt was made to extract resistors using the HBT technology file for Magic. The configuration of the HBT within Magic and the methods used for resistance extraction offer ways to extract HSPICE netlists for accurate simulations.

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